

ADQ7-FW2DDC configuration App Note



ADQ7-FW2DDC: application-specific firmware for radio systems:

- *Digital Down-Conversion*
- *Decimation*
- *Streaming data*
- *Multi-channel synchronization*
- *Differential / single-ended input*
- *2 analog inputs*
- *2 digital radio channels*

Applications:

- *RF system*
- *Channel sounder*
- *RF recording*
- *Satellite monitoring*
- *Radar*
- *Semiconductor RF test*
- *Spectrum monitoring*
- *Test and measurement*
- *RF production test*
- *5G*

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1 Introduction to ADQ7-FW2DDC

1.1 About this document

This document contains a description of the firmware option ADQ7-FW2DDC for the digitizer hardware platforms ADQ7DC and ADQ7WB. The focus of the document is on the firmware FW2DDC and its configurations and applications.

Read [Section 2](#) to see the basic configurations of ADQ7-FW2DDC.

Read [Section 3](#) to see the fundamental signal processing aspect of various configurations.

Read [Section 4](#) for a detailed description of each block in the design.

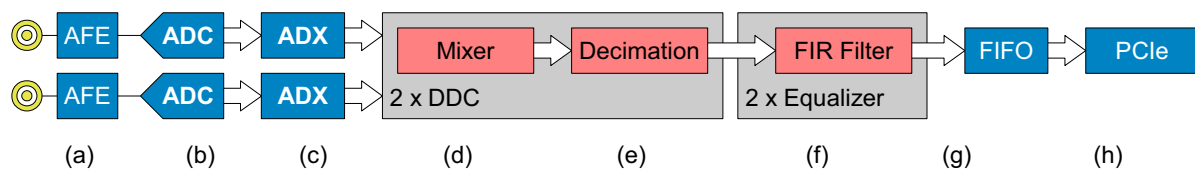
Read [Section 5](#) for a description of how to integrate hardware ADQ7 and the firmware FW2DDC in a system design.

Read [Section 6](#) for application examples and use cases.

A block diagram is in [Section 1.2](#) and definitions are in [Section 1.3](#) to [Section 1.6](#).

1.2 Block diagram of ADQ7-FW2DDC

The ADQ7-FW2DDC firmware option implements digital down-converters in the FPGA of an ADQ7 digitizer for a general purpose radio architecture. The structure of the ADQ7-FW2DDC is shown in [Figure 1](#).



#	DESCRIPTION	FURTHER READING	REF
a	There are 2 analog inputs for receiving either, I and Q, 2 RF channels, or a differential RF signal. The AFE on ADQ7DC is DC-coupled and optimized for the signal band 0 – 2.5 GHz. The AFE on ADQ7WB is AC-coupled and optimized for the signal band 1 – 6 GHz.	[3] , [4]	5.1
b	The high performance A/D converters are interleaved to reach higher instantaneous bandwidth.	[1] , [2]	4.2
c	ADX is SP Devices proprietary IP for interleaving correction of A/D converters which enable the unique wideband performance of ADQ7.		4.2
d	The quadrature mixer transforms the center frequency of the RF signal to the pass-band of the decimation filters.	[5] , [6]	4.4
e	The decimation reduces the sampling frequency and increase SNR in the signal band.	[5] , [6]	4.5
f	The general FIR filter is a user-defined filter for implementing an equalizer or IQ balance.	[5] , [6]	4.6
g	The FIFO handles the conversion from the real-time radio and the interrupt-controlled PC.	[3] , [4]	5.2
h	Connection to the host PC is done through a Gen3x8 PCIe interface.	[3] , [4]	5.3

Figure 1: Principle of the ADQ7-FW2DDC.

1.3 Definitions

The notation ADQ7-FW2DDC refers to the firmware installed on the hardware platform ADQ7. ADQ7 is then a collective name for the hardware products ADQ7WB and ADQ7DC. The notation FW2DDC refer only to the firmware and is used instead of ADQ7-FW2DDC when it is more suitable. The ADQ7-

FW2DDC firmware is controlled by a number of parameters. The definition and meaning of these parameters are defined in [Table 1](#).

Table 1: Parameters

	ACRONYM	UNIT	DESCRIPTION
General signal properties in digital and analog domain			
In-phase	I		Real part of a complex signal representation $i + jQ$. The term is used for both analog and digital signals.
Quadrature	Q		Imaginary part of a complex signal representation $i + jQ$. The term is used for both analog and digital signals.
Center frequency	fc		The center frequency of the signal band.
Bandwidth	BW		The bandwidth of the signal of interest. This is symmetrically placed around the center frequency.
Intermediate frequency	IF		A center frequency for the signal at an intermediate stage in a radio system. From the perspective of FW2DDC, RF and IF are identical.
Radio frequency	RF		A carrier (center) frequency used for transmission through the media. From the perspective of FW2DDC, RF and IF are identical.
zero-IF			Carrier (center) frequency is 0. This is used with complex signal representation $(I+jQ)$. This may be a property of the signal at the input of the ADQ7. The output of the DDC is almost always zero-IF.
Analog input			
Analog bandwidth	ABW	[Hz]	The analog bandwidth at the input of the digitizer. This is the frequency band within which the analog input signal has to be placed.
Nyquist band		[Hz]	This refer to the frequencies where aliasing do not occur. The width of one Nyquist band is equal to the sampling rate divided by two. The bandwidth of the input signal has to be located within one Nyquist band to avoid aliasing.
Mixer			
NCO frequency		[Hz]	Numerically controlled oscillator. Digital implementation of the local oscillator for the DDC. The frequency of the NCO sets the down-conversion. This is often set to $-fc$, to place the output signal around 0 and minimize the output signal bandwidth.
Decimation			
Decimation factor	N	[Hz]	Decimation factor sets the bandwidth. N is the number of decimation stages. The bandwidth reduction is 2^N .

1.4 About RF and IF

The terms RF and IF are used in this document. In the radio receiver system, the term RF denotes the signal used for transmission and the term IF is a local signal inside the radio.

In a system using IF, the RF is typically at a very high center frequency. The RF is down-converted by an analog mixer to a IF which is sampled by the digitizer.

In systems where the RF is a frequency within the analog input bandwidth of the ADQ7, the RF can be digitized directly.

Both RF and IF represent a signal with a center frequency and a defined bandwidth around that center frequency, **Figure 2**. It is even so that IF in one system can be at a higher frequency than the RF in another frequency. In summary; from the perspective of ADQ7-FW2DDC, an RF signal and an IF signal are identical.

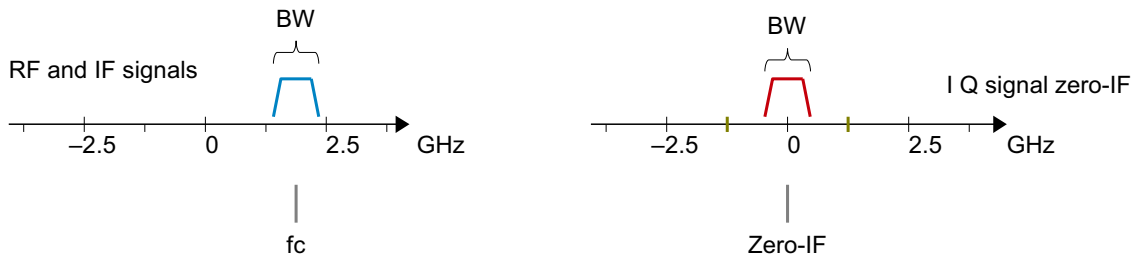


Figure 2: ADQ7-FW2DDC signal properties RF, IF, IQ, zero-IF.

1.5 Special case Zero-IF and IQ signaling

There is a special situation with IF frequency where the RF signal is down-converted to an IF at 0 Hz in the analog mixer before ADQ7, **Figure 2**. This situation requires analog I and Q complex representation of the analog signal.

In this situation, the I and the Q signal are fed to the two inputs of the ADQ7 hardware. The FW2DDC treat the two channels as I and Q. In this situation, the NCO should be set set to zero.

I and Q input may also be at a center frequency that is non-zero. The FW2DDC NCO is then set to this center frequency so that the output is zero-IF.

1.6 Output signal format I and Q

The output data from the FW2DDC is always a complex representation with In-phase (I) and Quadrature (Q) signaling on two separate digital data streams.

An analog signal with bandwidth 100 MHz at an IF is then down-converted by the FW2DDC to a zero-IF in I and Q representation. The sampling rate required is $f_s > 2 \times ABW$, that is $f_s > 200$ MHz. The I and Q representation mean that the data rate on I is >100 MHz and on Q is >100 MHz. So instead of one data stream at 200 MSPS we have two data streams at 100 MSPS each.

2 Configuration options block diagrams

There are several ways of configuring the ADQ7-FW2DDC for various types of radio applications. Below are the main configurations shown as block diagrams. The frequency planning view of these configurations are in [Section 3](#). These configurations are building blocks of the application examples in [Section 6](#). The details of the components in these block diagrams are in [Section 4](#).

2.1 I and Q receiver at an IF or zero-IF

The two inputs of the ADQ7 are treated as I and Q signals. The quadrature mixer in each DDC is then set up with complex input and complex output. [Figure 3](#) illustrates the configuration with one of the DDCs activated. The other DDC can be connected in parallel to this DDC and set up individually for a second radio channel. [Section 2.4](#) describe the use of multiple DDCs.

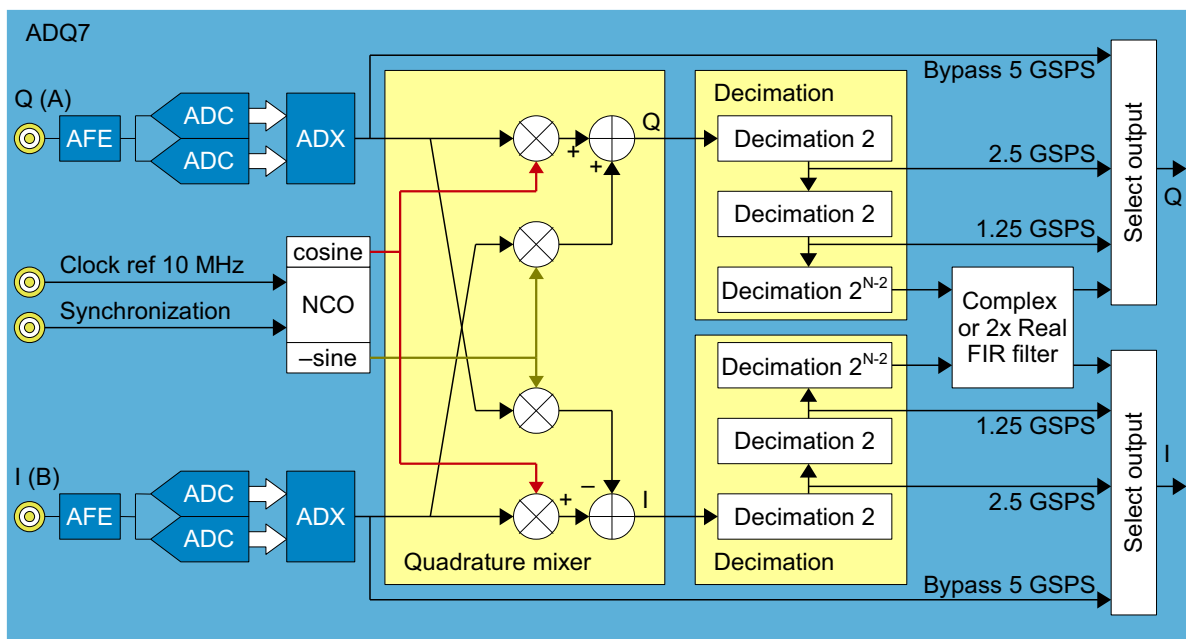


Figure 3: ADQ7-FW2DDC configured as wide-band I and Q receiver.

2.2 Dual input IF/RF receiver

The two inputs of the ADQ7 are considered to be two individual signals. This could be two antennas or two polarizations. The quadrature mixer in each DDC is then set up with real valued input and complex output. [Figure 4](#) illustrates the configuration with one DDCs activated per analog input channel. The two DDCs can be set up individually for two individual radio channels as output. The clock reference and synchronization are shared for both DDCs. The NCO frequency and the decimation factor is set individually so that each DDC can select a different center frequency and a different bandwidth. [Section 2.4](#) describe the use of both DDCs.

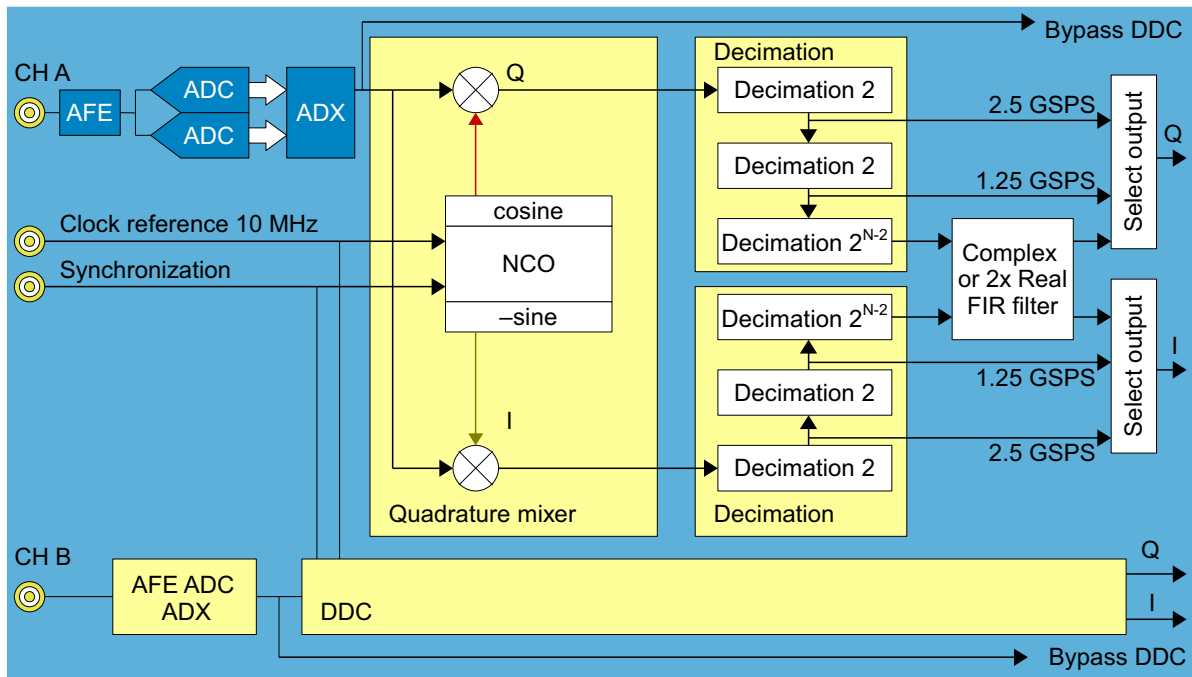


Figure 4: ADQ7-FW2DDC configured as two RF channels.

2.3 Differential input

The ADQ7 hardware has two single-ended inputs. These inputs can be used as a differential input with the value Channel A – Channel B as input to the DDCs, [Figure 6](#). The difference Channel A – Channel B is considered a real valued input.

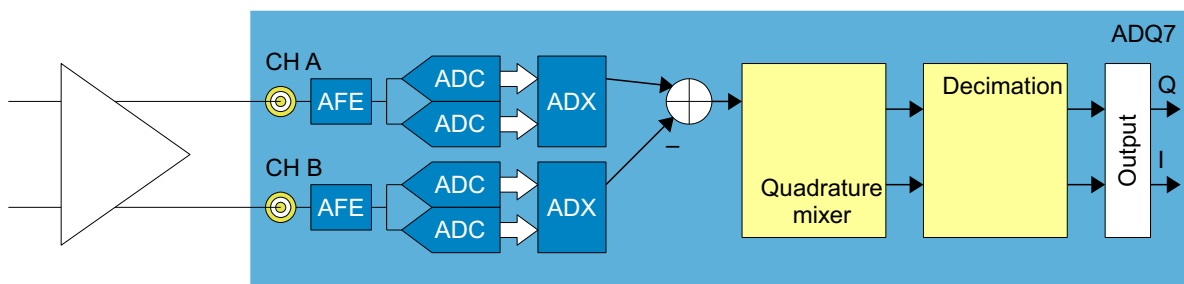


Figure 5: ADQ7-FW2DDC differential

2.4 Two output channels

A cross-point switch connects the two analog inputs to the two DDCs, [Figure 6](#). See [\[6\]](#) for details on how to set up the cross-point switch.

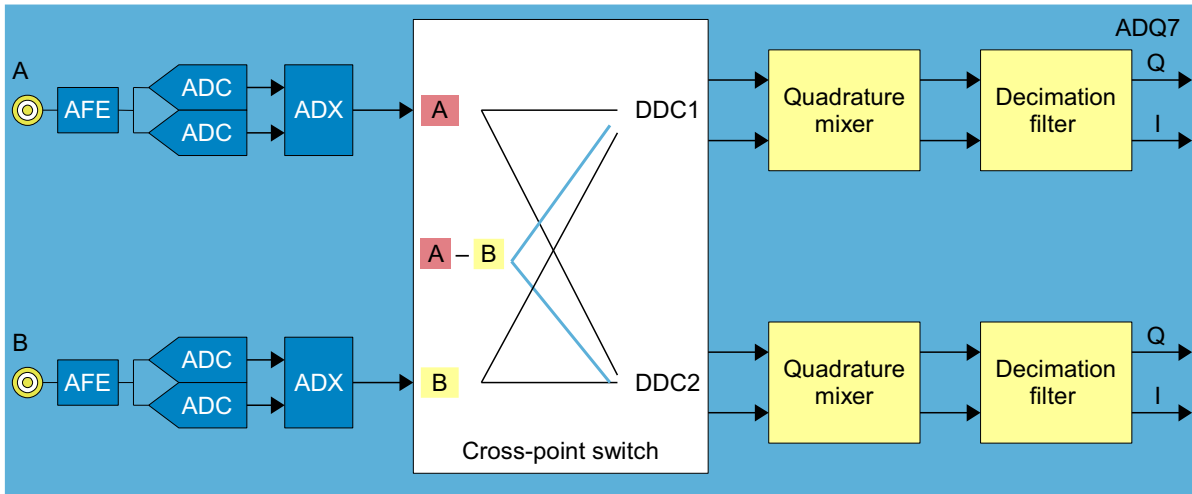


Figure 6: ADQ7-FW2DDC cross-point switch

3 Signal processing case

3.1 IQ zero-IF receiver

The analog input has an I and Q representation and a zero-IF modulation. This means that the signal is placed around 0 Hz. Use the bypass function to capture full bandwidth. If the signal bandwidth is lower, it is possible to bypass the quadrature mixer and use only the decimation functions in order to optimize data rate to host the PC.

The analog signal bandwidth can be up to 5 GHz with IQ-representation. The data rate will be up to 20 GBytes/s, so recording into ADQ-DRAM is required. This means a triggered application where a time slot of up to 200 ms is recorded per trigger.

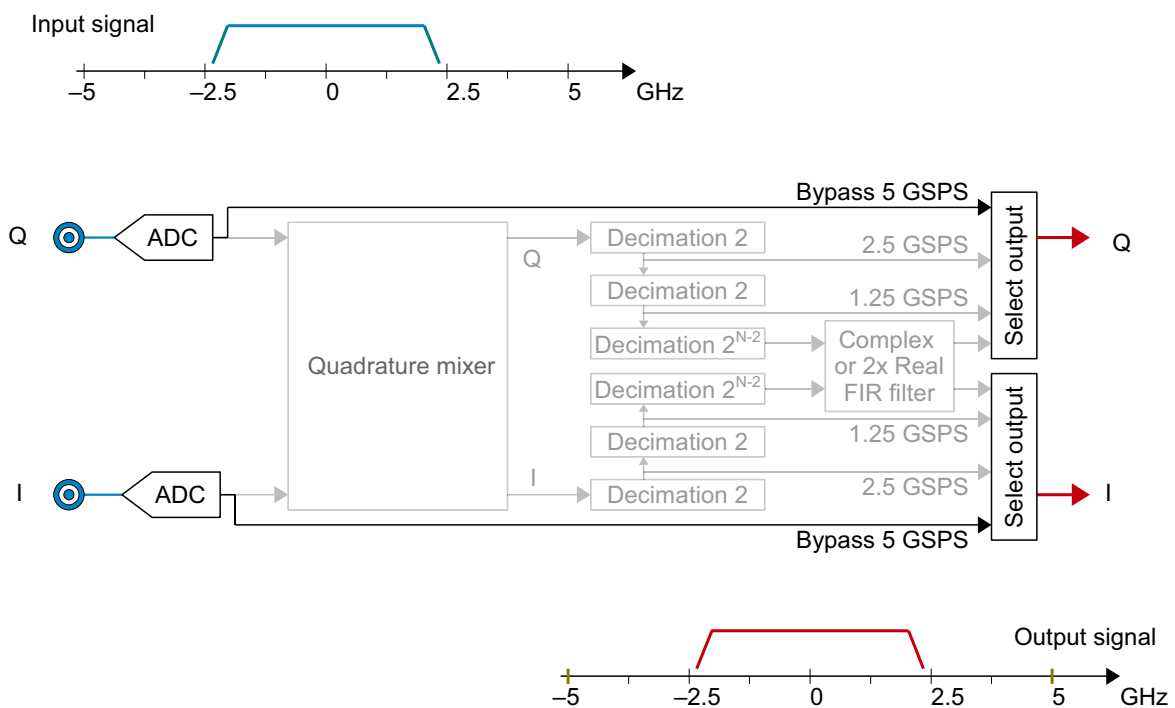


Figure 7: ADQ7-FW2DDC configured as wideband zero-IF I and Q receiver.

3.2 IQ low-IF receiver

The analog input has an I and Q representation and an IF modulation. Use the quadrature mixer to down-convert the signal to zero-IF. The decimation of the individual I and Q branches changes the data rate from 2 x 5 GSPS to 2 x 2.5 GSPS. This is possible since the output signal is placed symmetrical around 0 Hz

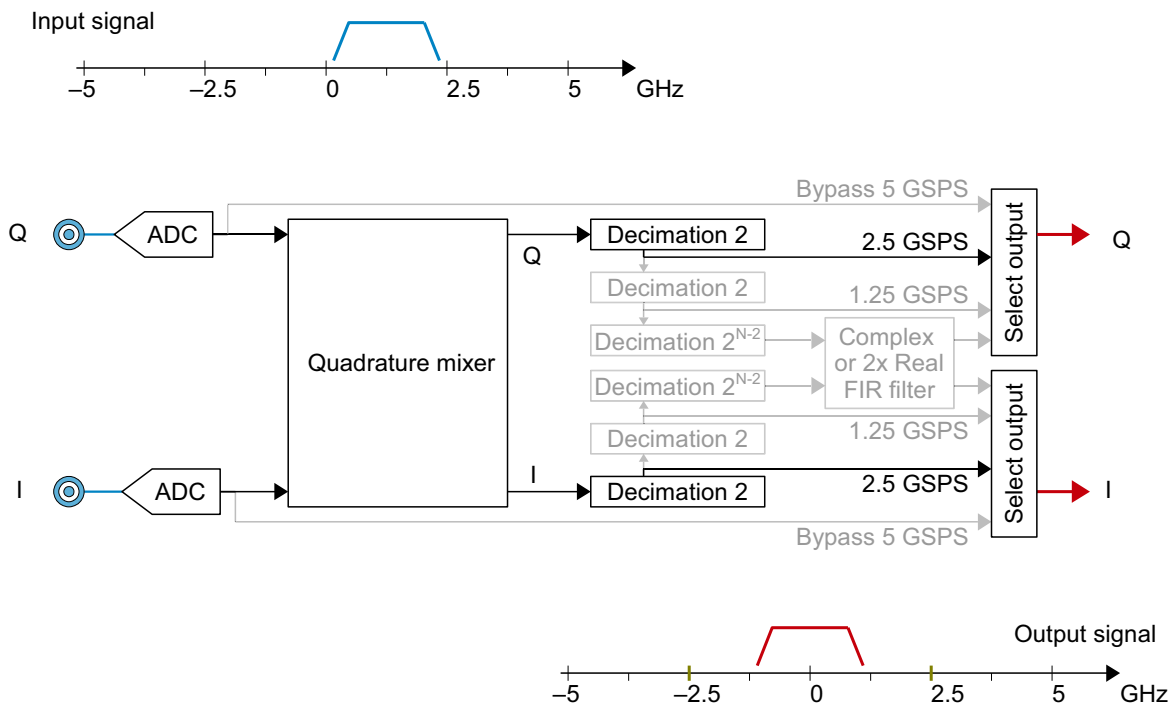


Figure 8: ADQ7-FW2DDC configured as wide-band zero-IF I and Q receiver.

3.3 Narrow-band IQ low-IF receiver

The analog input has an I and Q representation and an IF modulation. Use the Quadrature mixer to down-convert the signal to zero-IF and use the decimation function to reduce the data rate. The example below illustrates a decimation factor $N=2$ meaning decimation of 4. The effective data rate is reduced a factor of 2 from 1×5 GSPS to 2×1.125 GSPS.

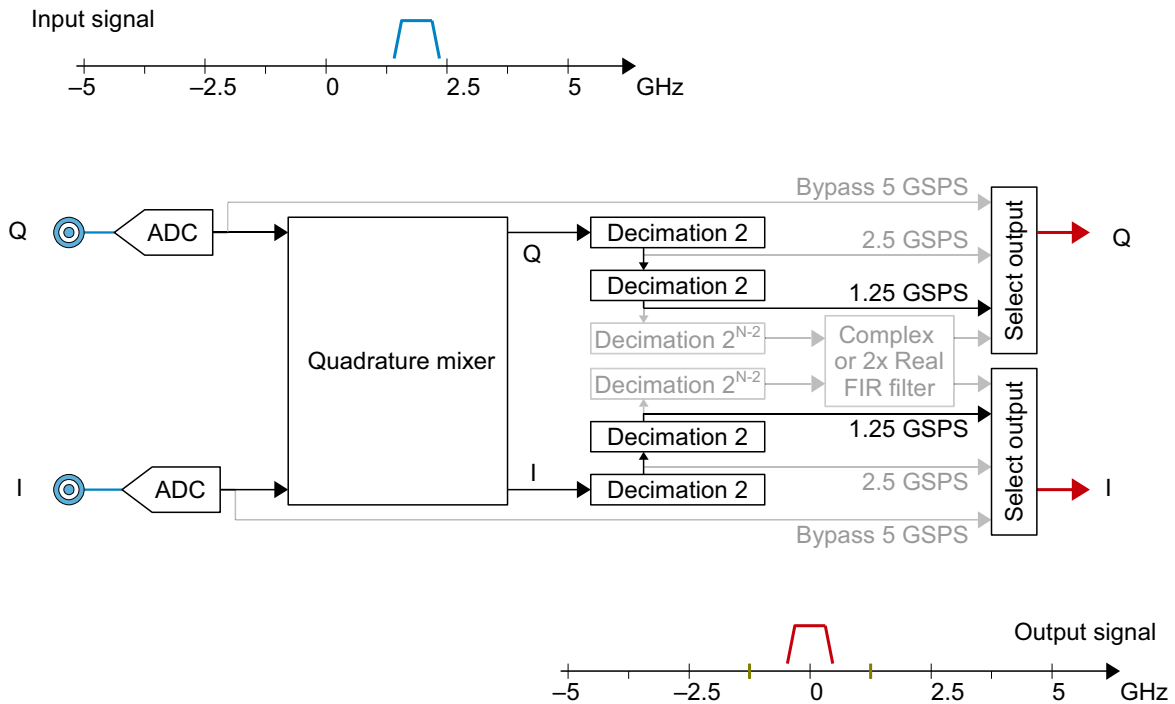


Figure 9: ADQ7-FW2DDC configured as a narrow-band low-IF I and Q receiver.

3.4 Wide-band real-valued low-IF receiver

The analog input has an real-valued representation and an IF modulation. Use the quadrature mixer to demodulate the signal to zero-IF and use the decimation function to reduce the data rate.

The channels are individual. Only one channel is shown below.

Note that the real-valued input sampled at 5 GSPS can represent an analog signal with a bandwidth of 2.5 GHz. When converted to I and Q in the quadrature mixer, the signal bands of I and Q are placed from -1.25 GHz to $+1.25$ GHz. This means that the two streams must have a sampling rate of 2.5 GSPS. The first stage of decimation is thus activated on the I and Q signals.

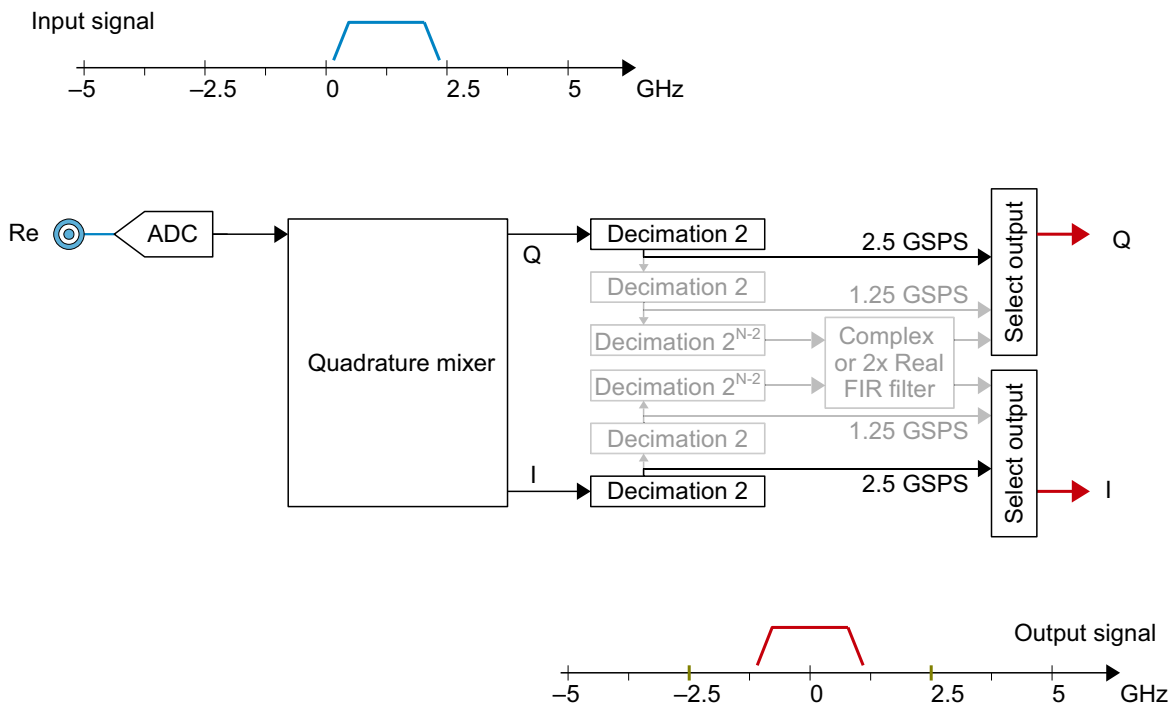


Figure 10: ADQ7-FW2DDC configured as a wide-band low-IF receiver. Only one of the channels is shown.

3.5 Narrow-band real-valued low-IF receiver

The analog input has a real-valued representation and an IF modulation. Use the quadrature mixer to demodulate the signal to zero-IF and use the decimation function to reduce the data rate.

The channels are individual. Only one channel is shown below.

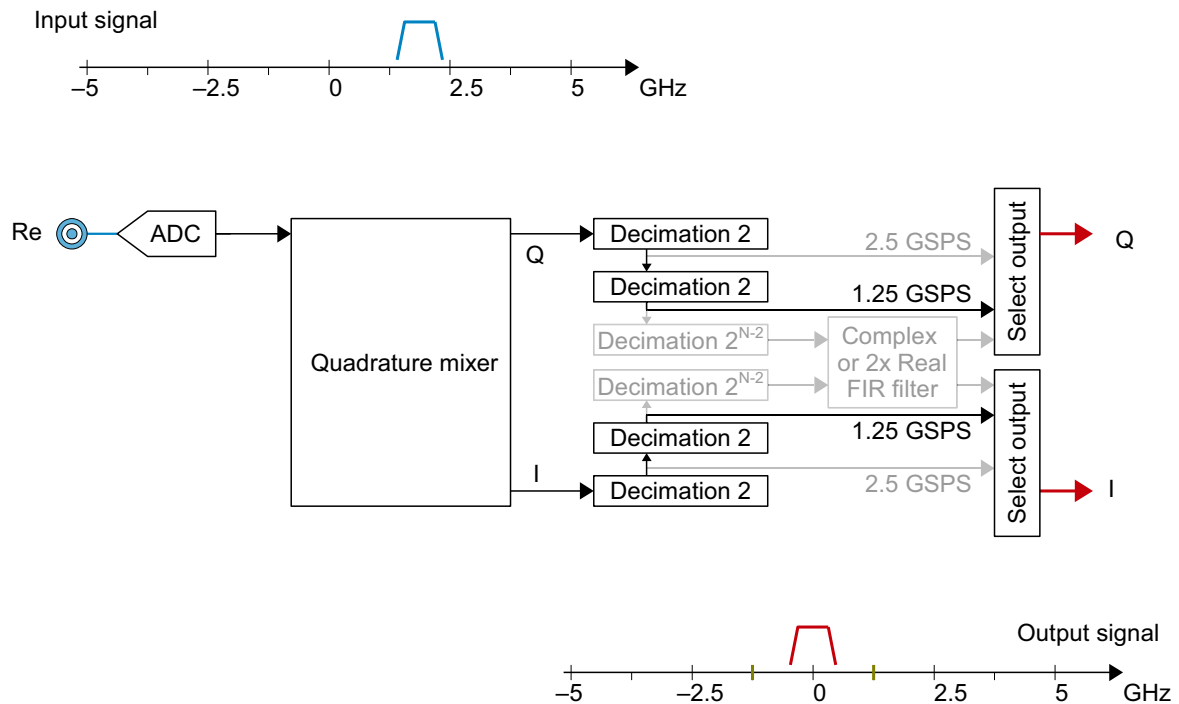


Figure 11: ADQ7-FW2DDC configured as a narrow-band low-IF receiver. Only one of the channels is shown.

3.6 Equalizer for real-valued low-IF receiver

The analog input has an real-valued representation and an IF modulation. Use the quadrature mixer to demodulate the signal to zero-IF and use the decimation function to reduce the data rate.

The ADQ7-FW2DDC has a decimation function with a programmable order from 1 to 2^{32} . If the decimation order is set larger than $2^3 = 8$ a general FIR filter can be activated. The general filter which can be configured either as a complex filter or as two independent filters. The data rate into the general filter is maximum 625 MSPS per I and Q, which means maximum analog bandwidth in the order of 500 MHz, that is from -250 MHz to $+250$ MHz.

The channels are individual. Only one channel is shown below. The arrows indicate the potential effect of an equalizer. The equalizer has to be tuned by the user in the target system.

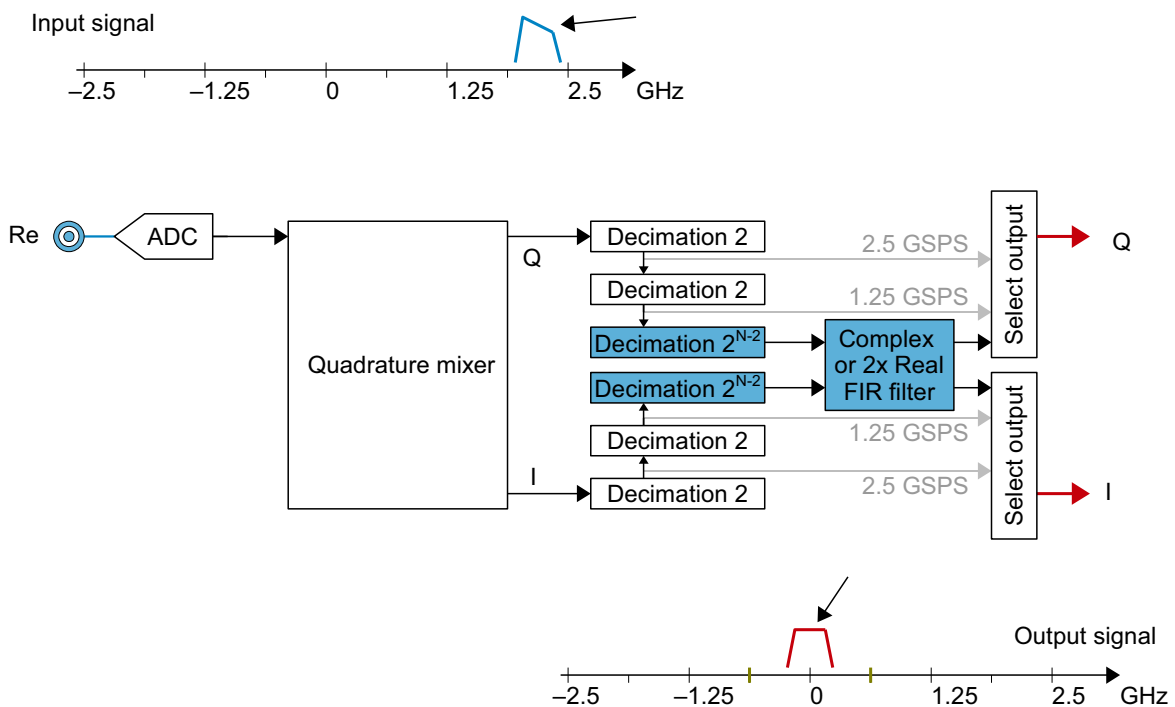


Figure 12: ADQ7-FW2DDC configured as a narrow-band low-IF receiver. Only one of the channels is shown. The arrows mark the effect of an equalizer.

4 Block description of FW2DDC

4.1 Selecting the clock frequency

The analog input of the ADQ7 support several Nyquist bands. The Nyquist bands are a function of the sampling frequency. To avoid aliasing, the complete analog bandwidth of the signal of interest has to fall within one Nyquist band. By selecting the sampling frequency, the Nyquist bands can be adjusted to the requested signal band. ADQ7 supports two modes of operation; 4 GSPS and 5 GSPS, **Figure 13**.

- When operating at 5 GSPS the Nyquist bands are 0 – 2.5, 2.5 – 5, 5 – 7.5¹.
- When operating at 4 GSPS, the Nyquist bands are 0 – 2, 2 – 4 and 4 – 6 GHz.

Figure 13 illustrates the selection of sampling frequency. For signals in the purple frequency bands, 5 GSPS has to be selected to avoid aliasing. For signals in the green frequency bands, 4 GSPS is required.

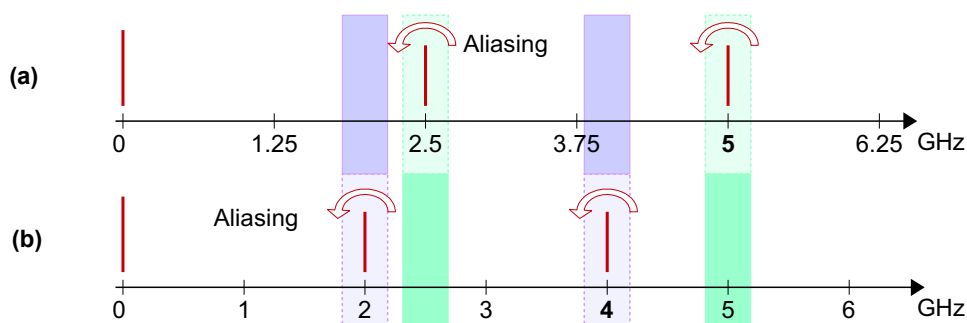


Figure 13: Select sampling rate depending on the analog signal band.
(a) using 5 GSPS enables the band around 2 GHz.
(b) using 4 GSPS enables the band around 2.5 GHz.

4.2 ADX interleaving correction

ADX is a proprietary technology from Teledyne SP Devices that improves the signal quality for a wide bandwidth. ADX eliminates the characteristic non-ideal effects of interleaving. ADX operates in the background and is automatically updating parameters using all available incoming signals.

The benefit from ADX is visible when the bandwidth of the channel is larger than $f_s/4$ or when the signal band is spanning across the frequency $f_s/4$. The effect of time-interleaving can be controlled by selecting the sampling frequency. By selecting 5 GSPS, the frequency where ADX is crucial to use is at 1.25 GHz. By selecting 4 GSPS, the critical frequency is 1 GHz.

ADX can operate in the first or second Nyquist band, **Figure 14**.

1. The Nyquist band is up to 7.5 GHz, but the analog input bandwidth is only up to 6.5 GHz.

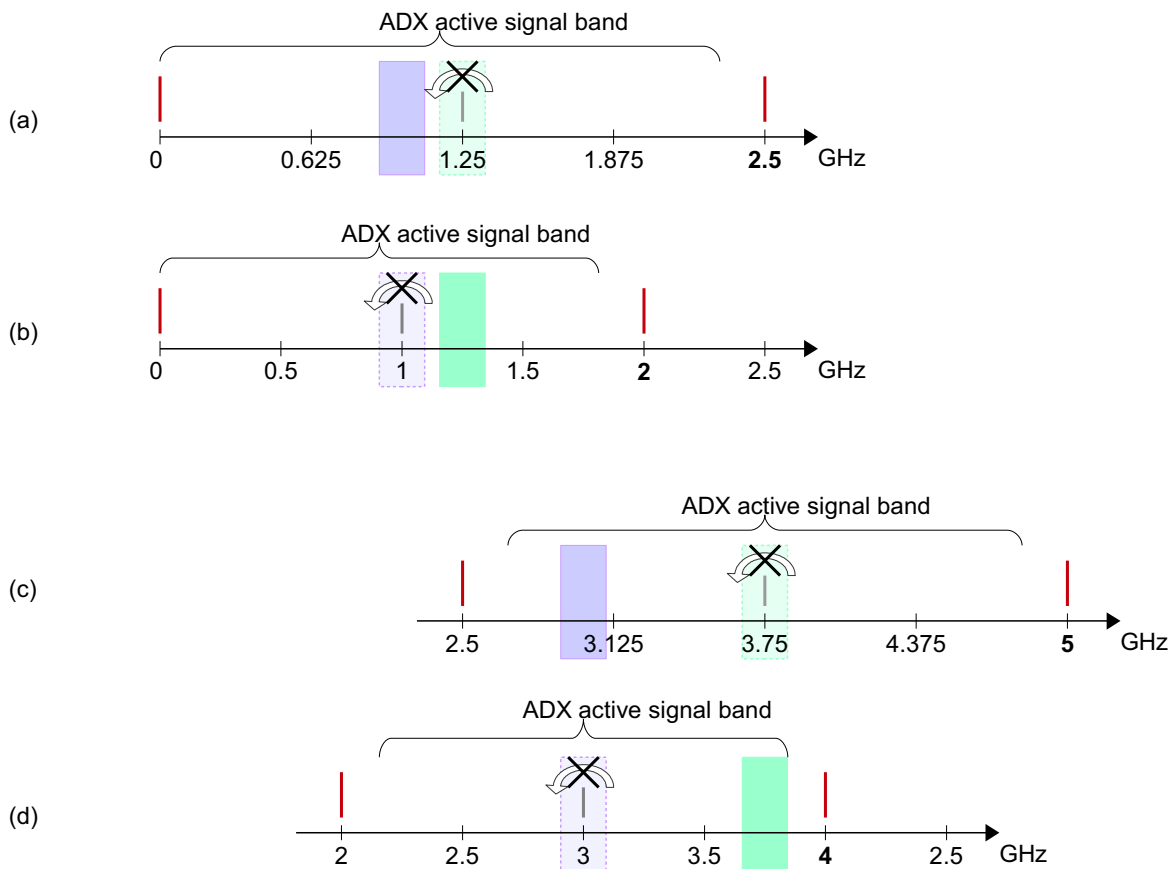


Figure 14: ADX eliminates aliasing.
(a) first Nyquist band when using 5 GSPS.
(b) first Nyquist band when using 4 GSPS
(c) second Nyquist band when using 5 GSPS.
(d) second Nyquist band when using 4 GSPS.

4.3 Digital Down Converter

The digital down converter consist of a quadrature mixer, [Section 4.4](#), and a decimation filter, [Section 4.5](#). There are two DDC on the ADQ7-FW2DDC. This means that two radio channels can be received simultaneously. See [Section 2.4](#) for on how to connect the DDCs to the respective digitized analog inputs. The DDCs can handle full bandwidth, which mean that can take deliver 2.5 GSPS on I and 2.5 GSPS on Q output. This correspond to a 2.5 GHz Nyquist bandwidth (± 1.25 GHz)¹.

4.4 Quadrature mixer

The quadrature mixer converts the signal frequency from the incoming signal band to the pass-band of the decimation filters. The Numerically Controlled Oscillator (NCO) operates as Local Oscillator (LO).

It is possible to use different frequencies on different digitizer channels in order to receive different frequency bands. It is also possible to control the phase of each NCO individually for phased array applications.

The preferred selection of the NCO frequency is to match the center frequency of the analog signal. This gives the tightest representation of the digital output. The signal band is placed symmetrical

1. In practice, the usable bandwidth is limited by the pass-band of the decimation filters to ± 1 GHz.

around 0 and the minimal sample rate can be used. The output bandwidth is then from $-ABW/2$ to $+ABW/2$.

If this is for some reason not possible, a different NCO frequency can be used. The result is that the digital output bandwidth is higher.

Example: Analog bandwidth 400 MHz, f_c at 1 GHz and NCO is set to -900 MHz. The analog input signal is in the band 800 to 1200 MHz. The digital output is then in the band -100 to $+300$ MHz. The sample rate has to be 625 MHz for a bandwidth of 500. If the NCO is set to match the f_c , that is 1 GHz, the output band is -200 to $+200$ MHz, the sample rate can be set to 312.5 for a bandwidth of 250 MHz

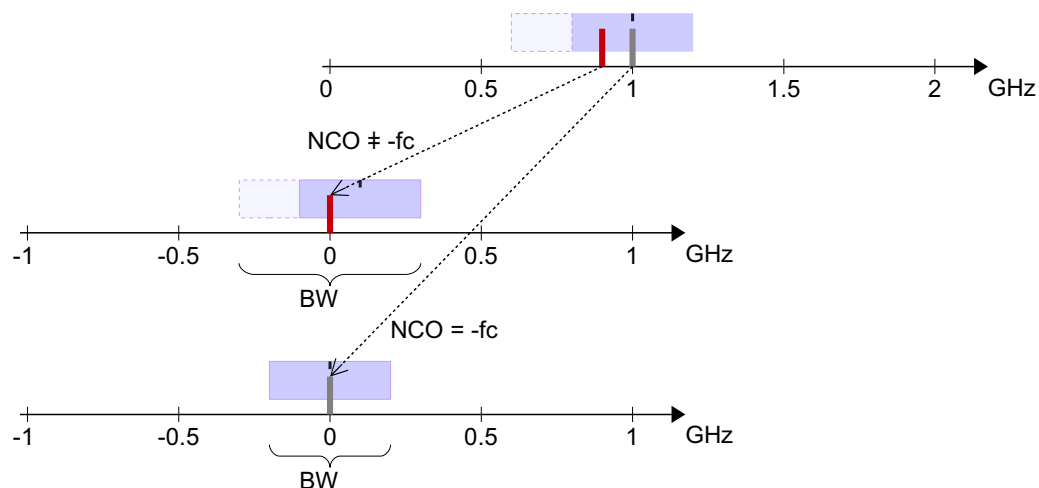


Figure 15: Selecting NCO frequency.

4.5 Decimation

The decimation block consists of a low pass filter structure and a sample rate reduction through sample skip, **Figure 16**. The low-pass filters reduce the signal bandwidth and also removes the high frequency noise. After the filters, sample skip can be applied without aliasing of the noise into the signal band. There is a large variety of radio system, so the order of decimation has a very wide range of settings (from bypass to 2^N).

The decimation filter is built up by a series of identical half-band FIR filters. See figures in **Section 2** and **Section 3** for a block diagrams of the decimation filter modules. Each filter reduces the signal bandwidth to 40% of the Nyquist band and thus allow for a sample rate reduction of a factor of 2.¹ Out from the first filters the data rate is very high. The outputs from these filters cannot be combined with the general FIR filter function. The following decimation stages are drawn as order 2^{N-2} , which means a series of $N-2$ identical decimations with a factor of 2 each. The output from these stages can be combined with general FIR filter.

High order of decimation increases the SNR. For decimation factors over $2^8 = 256$ it may be beneficial to change from 16 bits to 32 bits representation².

The decimation factor is individual for each channel.

1. The pass band is 40% of the incoming signal band and thus 80% of the outgoing signal band at half the sample rate.
2. A decimation factor of 256 is fully realistic. If the sampling rate is 5 GSPS this decimation factor means 19,53 MSPS and a signal band width close to 10 MHz, which is a realistic radio channel. Also when studying distortion, **Section 6.5**, small bands are studied with high precision.

Example: The sample rate in the decimation stages is a series; 5 GSPS, 2.5 GSPS, 1.25 GSPS... This is designed to match and instantaneous bandwidth of; 2 GHz, 1 GHz, 0.5 GHz... The theoretical bandwidth is up to the Nyquist frequency, but there has to be transition band for the filters, which reduces the bandwidth to 80 %.

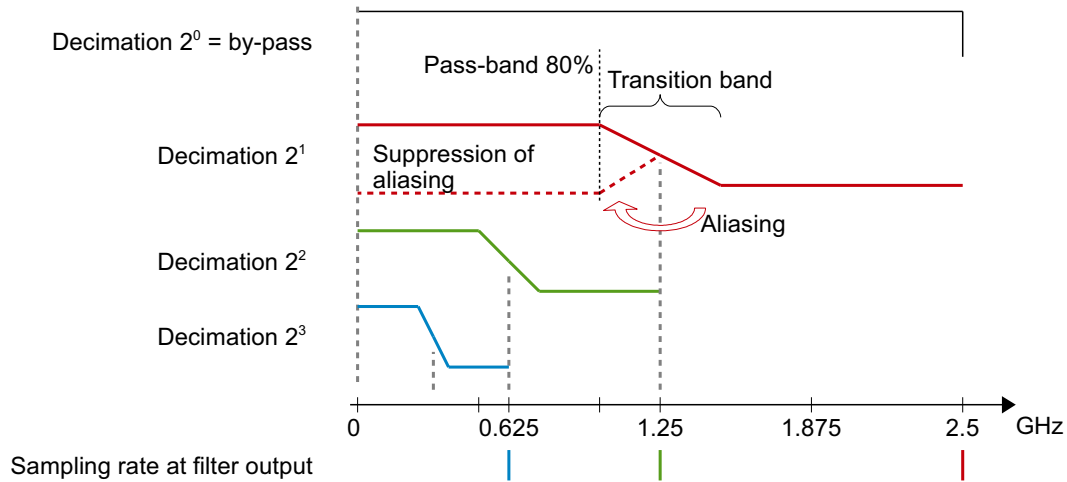


Figure 16: Decimation properties.

4.6 Filter, Equalizer or IQ balance FIR structure

After the decimation filter is a general-purpose FIR-filter with user-controlled coefficients. The filter may be configured as two individual real valued filter or a complex FIR filter.

When configured as two real-valued FIR filter it can be used as equalizers. The position in the signal chain (after decimation) means that it will equalize the signal band of interest only. The equalizer may then be realized with a short filter. By configuring the filter as a complex FIR, it can be used for IQ-balancing.

The data rate into the filter is set by the selected decimation and is maximum 625 MSPS.

5 System design using ADQ7-FW2DDC

5.1 Analog front end considerations

The core parameters of the analog input are the bandwidth of the analog signal and the center frequency of the analog signal. These has to fall within the bandwidth of the analog input. The ADQ7 contains 2 hardware platforms, ADQ7DC and ADQ7WB. The selection of hardware platform is related to analog input signal frequency:

The analog front-end is AC-coupled on ADQ7WB. This is intended for high frequency applications, since the linearity is optimized at high frequencies. The ADQ7WB is preferred if the main signal energy is above 1 GHz.

The DC-coupled front-end on ADQ7DC is intended for a Zero-IF systems. The DC coupled front end is designed for highest dynamic range at low frequencies. ADQ7DC is preferred if the highest frequency is below 1 GHz.

More information about the hardware platforms are in the respective datasheets; [1] and [2].

5.2 On-board DRAM as FIFO.

The data stream from the FW2DDC is real-time, which means that it is controlled by the events like triggers. To handle the non-real-time behavior in the host PC, there is a 4 GBytes data FIFO on the ADQ7. The FIFO guarantee reliable data transfer at a high sustained rate over long time.

This FIFO is also used for batch wise recording. The ADQ7 can produce up to 20 GBytes/s of data. The PCIe interface to the host PC is limited to about 7 GBPS¹. This means that bursts of data can be recorder into the DRAM at full speed, and then be read out to the PC at lower speed.

Note that the possible setting of the DDCs do not exceed the bandwidth to the DRAM of 20 GBytes/s.

5.3 PC host interface

The interface to the host PC is using the PCIe communication standard. The capacity is generation 3 by 8 lanes, which means a bit rate of 64 GBits/s. The physical interface is either PXIe or PCIe. The ADQ7-FW2DDC supports record based acquisition and continuous streaming to the host PC.

5.4 Acquisition mode Continuous streaming.

Continuous streaming means that there is a continuous flow of data from the start until the end of the measurement, [Figure 17](#). The data is one long single recording which continue until it is terminated by the user.

To use continuous streaming, the data rate has to be adopted to the host PC interface by appropriate decimation. The maximum capacity is determined by the ADQ7 in combination with the host PC and possibly also the disk write speed. ADQ7 hardware support Gen 3 by 8 PCIe interface to the host PC. Such an interface typically deliver 5 to 7 GBytes/s depending on the PC set-up.

Example: The minimum data rate required by the application is double the signal bandwidth. (In practice, a little margin is required for filters.) For example, a 50 MHz signal requires 100 MSPS minimum sample rate. The pass-band of the decimation filter is 80% of Nyquist frequency, so in practice $100/0.8 = 125$ MSPS is the minimum. For an I and Q zero-IF representation, this means minimum 62.5 MSPS on I and Q branch. The decimation filters can be set in power of 2, that is, 2, 4, 8 and so on. Set the decimation factor to $2^6 = 64$ to get $5000/64 = 78.125$ MSPS per I and Q branch. (For definition of I and Q, see [Figure 12](#).) Each sample is 2 bytes. Thus I and Q together will result in $78.125 \text{ MSPS} \times 2 \text{ bytes/sample} \times 2 = 312.5$ MBytes per second data rate to the PC.

1. The exact speed limit depend on the entire system.

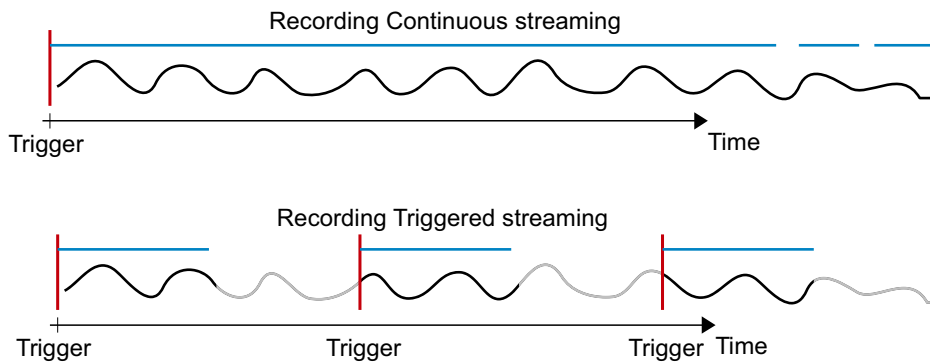


Figure 17: Streaming modes.

5.5 Acquisition mode Triggered streaming

Triggered streaming means that associated to each trigger event is a record of data with a pre-determined recording time, **Figure 17**. Each record contains a header with time-stamp of the trigger time and a record number.

For a continuous stream of triggered records, the average data rate is then *Record Length X Trigger Rate*. Thus data rate to the PC is controlled by these parameters. Set the combination of record length and trigger rate to match the capacity of the host PC.

Triggered streaming is used for burst recording. The on-board DRAM on the card then work as a FIFO to store the high speed bursts before transmitting the data to the PC: In this way a, a peak data rate can which is much higher that the PCIe data rate can be recorded. The system is independent of the data rate to the PC if the total amount of data *Record Length X Number of Records* fits into the DRAM of 4 GBytes. If the total data set is larger, the average recording data rate has to be lower than the host PC

5.6 Connecting to a host PC for processing or storage

Use the ADQ7-FW2DDC signal processing capability to adjust the data rate. The data rate has to match the signal bandwidth according to the sampling theorem. The data rate in the transfer to the PC is above 5 GBytes/s. The ADQAPI supports data transfer to user's buffers in the API, **Figure 18**. From those buffers, the application software¹ can use the data or store it on a disk.

1. Application software is designed and implemented by the user.

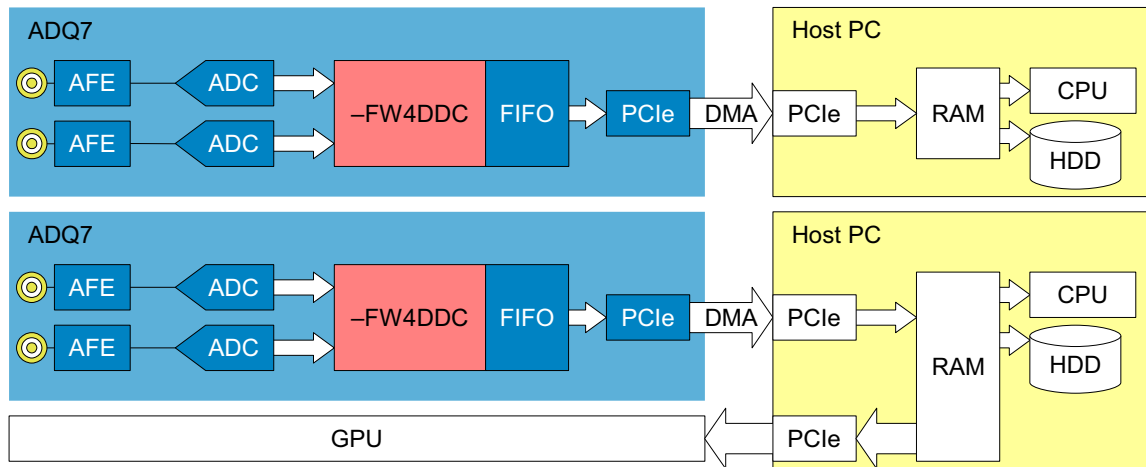


Figure 18: Streaming data to CPU or GPU.

5.7 Streaming to GPU

The hardware in ADQ7 supports peer-to-peer streaming to GPU at up to 7 GBytes/s from FWDAQ. Streaming from FW2DDC is via the host PC, **Figure 18**. The software to stream from the PC RAM to the GPU is a part of the user's application.

Data is also sent in packages. Even if it is a continuous stream of samples, a packet size has to be assigned and the data is transferred in these packages. The seamless data stream is then available in a series of buffers in the GPU.

5.8 Synchronization to analog mixer by phase locking the NCO.

The NCOs can be phase locked to the external (or internal) 10 MHz clock reference. This is done by setting up the system similar to **Figure 19**.

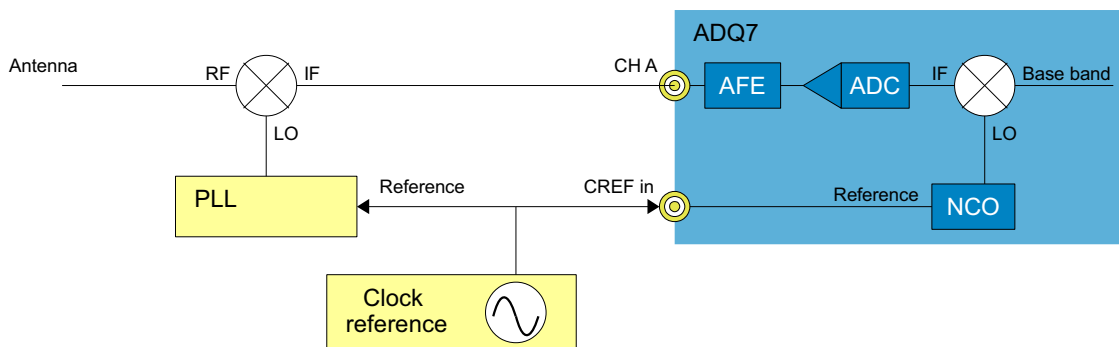


Figure 19: Principle of clock reference distribution

The NCOs in the ADQ7 can be locked to the clock reference as in **Figure 20**. Set up the digitizer to wait for an external SYNC signal¹. The NCOs are phase locked to 10 MHz reference at the clock edge following after the sync signal. Time-stamp is also reset with this signal.

1. The external trigger may also be used. This is set by a software command.

The phase and frequency of each NCO is set individually, which is useful for phased array applications.

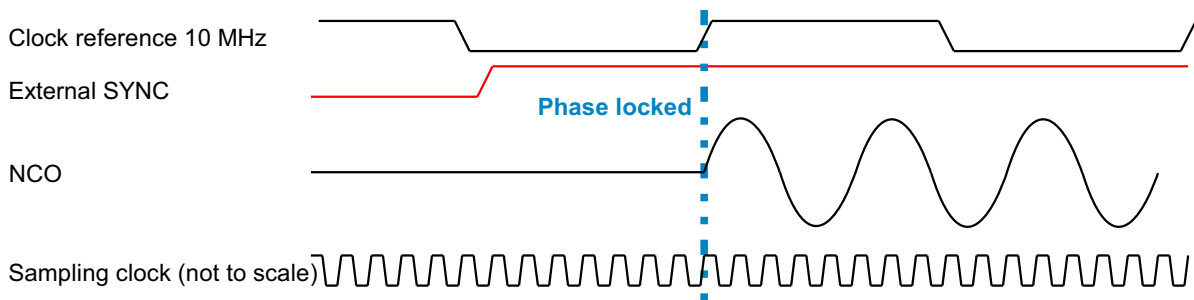


Figure 20: Phase lock to external 10 MHz reference

5.9 Synchronizing several ADQ7-FW2DDC to each other.

By distributing the SYNC signal and the clock reference to several ADQ7-FW2DDC, fully synchronous multi-channel system is achieved.

5.10 Synchronized acquisition start.

Both acquisition modes, [Section 5.4](#), are started with a trigger event. When using the phase lock function of [Section 5.8](#), all triggers are blocked until the synchronization is completed. Then the acquisition will start on the first trigger.

6 Application examples

6.1 Fundamental application; RF recording

The fundamental application for ADQ7-FW2DDC is an RF recording system. An RF / IF or IQ signal with a specified bandwidth and center frequency is acquired by the ADQ7. The FW2DDC use the NCOs and mixers converts the center frequency to 0 or a low frequency. The decimation filter limit the bandwidth and the sample rate to fit the input signal. This down-converted signal is then streamed to a PC or a GPU via the PCIe interface.

This fundamental function is a basis for all the following applications. The summary in bullet form of the implementation of RF recording is:

- The wide-band analog input allow the analog signal to be placed at an optimal center frequency.
- Use the DDC to select a center frequency and a bandwidth of interest.
- Use the high speed PCIe data link to send the data to the host PC.

The standard product ADQ7-FW2DDC delivers data is buffers in the PC RAM. The en user's application software stores the data to a selected media.

6.2 Wide-band time-slot recording

This is an variant of the RF recording and is valid when the recording data rate is higher than the data rate to the host PC. When the bandwidth of the analog signal is so high that the peak data rate is too high for direct streaming to the PC. A time-slotted recording using triggered streaming is a solution. The DRAM of the board act as a FIFO to transform the peak data rate at the recording to a lower data rate that can be transferred to the host PC. The blocks in time-slot recording are:

- The signal can be an RF / IF signal or and IQ signal. If the input signal is IQ with zero-IF, the actual bandwidth that can be recorded is 5 GHz.
- At each trigger (time-slot start) a batch of data (record) of full bandwidth is recorded into the DRAM.
- Use the triggered streaming interface for a immediate data transfer to the host PC.

This system can be used to reach 25% duty cycle at a 5 GHz analog bandwidth. The time slots are up to 200 ms. The timing diagram is in [Figure 21](#).

In this way, very wide band signals can be studied. This is useful for, for example, studying distortion, where a high number of harmonics is required. In the special situation where the analog signal is complex I and Q with zero IF, the recorded signal band is +/- 2.5 GHz = 5 GHz. In a general situation, the analog bandwidth is above 6 GHz, but the Nyquist band is only 2.5 GHz (at 5 GSPS). This means that high order distortion will be aliased into the signal band. By placing the fundamental at proper for frequencies, the harmonics do not fold on top of each other and they can still be distinguished.

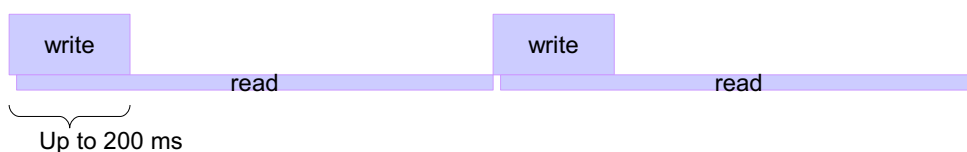


Figure 21: ADQ7-FW2DDC batch wise recording at full speed to DRAM.

6.3 Frequency band surveillance

The frequency surveillance application is to monitor a certain frequency band and alert when there is activity of a certain type. This method is applicable in many areas where the most natural is signals intelligence or frequency band monitoring. This can, however, also be used in test equipment for fault detection of rare events. The ADQ7-FW2DDC contributes to this application in four main ways:

- The wide analog input bandwidth allows for receiving a large frequency band. When the full analog bandwidth is available at the digitizer input the frequency band selection is moved to the digital domain. The hardware design can then remain the same and the system is very dynamic.
- The DDC select a sub-band to analyze. To monitor the entire analog frequency band of 0 to 6 GHz is seldom required. A too large bandwidth also adds unnecessary computational burden on the PC system. The DDC optimize the frequency selection. Using several DDC means that several sub-bands can be studied simultaneously. The DDC can be re-tuned instantaneously to another center frequency and another bandwidth to follow activity in the radio channel.
- The streaming interface is designed for continuous operation. Once set up, the streaming of data can continue 24 / 7 without reconfiguration. The streaming interface handles triggered records and continuous data. The data rate on each channel can be adopted to each channels needs.
- The computation and analysis of data is done in a user's software. The ADQAPI is an open interface for optimal control of the digitizer and the data flow. The ADQAPI allows for designing high speed real-time systems.

Note that FFT software and frequency trigger is a part of the user's application and not included with FW2DDC.

6.4 Frequency Pattern Recognition

The ADQ7-FW2DDC is the backbone data recording solution for an automatic frequency pattern recognition application. The wide band recording and streaming to GPU build up the core data flow of the application. Then apply ML algorithms to identify objects.

Note that ML software is a part of the user's application and not included with FW2DDC.

6.5 Automated test system

The ADQ7 is also designed for integration in an automated test system. The performance and features of the recording naturally supports many types of test systems. The open API allows full automated control of all features of the digitizer from an application software. The triggered streaming interface allows for 24 / 7 high speed operation in a real time system.

The flexibility of ADQ7-FW2DDC enables switching between different tasks during runtime. Use the bypass function to record time domain data, then activate the DDCs to study a certain frequency band. It is also possible to set one DDC in bypass mode and activate another DDC to get both time domain raw data a certain selected frequency band at the same time.

The ADQ7 can be used both for verification tasks by logging performance and for fault detection by alerting on deviations from expected performance.

Test system frequency detection

By streaming data to a host and combining it with an FFT and a frequency trigger mask, the ADQ7 can be used for fault detection of an RF system.

Test system distortion measurement

Use the high analog input bandwidth to measure distortion as in [Figure 22](#). By selecting a proper fundamental frequency an an appropriate sample rate, the harmonics are aliased in a way that they can be distinguished.

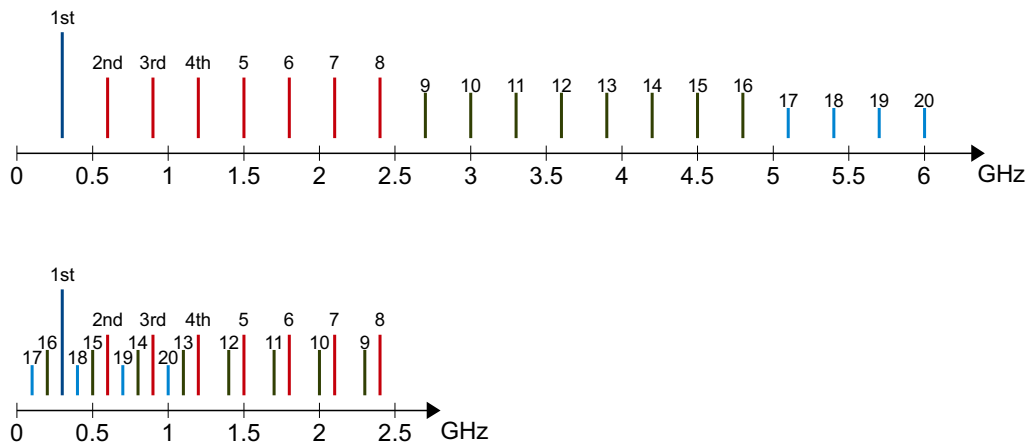


Figure 22: ADQ7-FW2DDC Measuring distortion up to 6 GHz. Analog frequency band and aliased digital frequency band.

6.6 Channel sounder

The synchronization features of the ADQ7 makes it suitable for channel sounder. Operating the ADQ7 at 4 GSPS mean a symbol correlation the SDR14TX. The clock reference input and the sync and TRIG trigger functions enables synchronization to the pattern of the source.

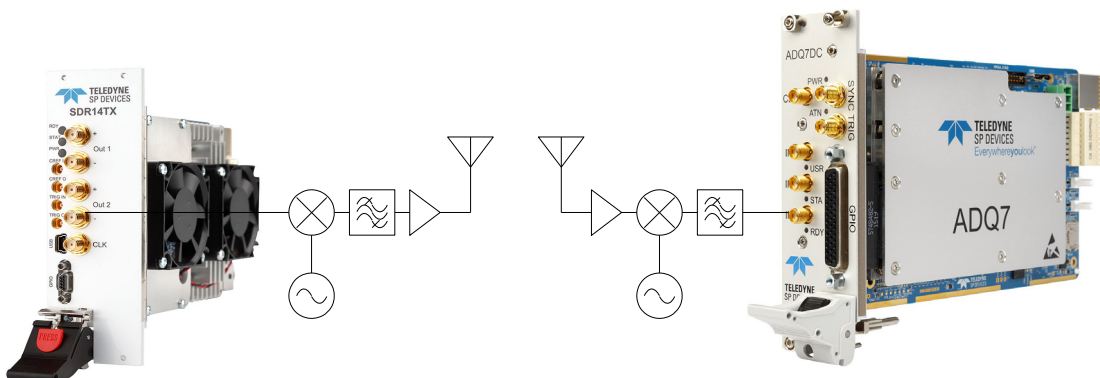


Figure 23: ADQ7-FW2DDC channel sounder system with SDR14TX as AWG.

6.7 Scientific instruments

The wide-band analog input of ADQ7 allows for a large variety of applications and detectors. Any system that is based on a center frequency and a determined bandwidth around that center frequency will benefit from the FW2DDC.

The PCIe form factor and the streaming capability of ADQ7 allow for an efficient high performance integration of the system. By streaming to GPU allows for a high performance analysis of the recorded data and also advanced Machine Learning applications.

Electron Paramagnetic Resonance EPR

The EPR system is recording a signal with a frequency band that is around a center frequency and has a determined bandwidth, which is in focus for ADQ7-FW2DDC.

Magnetic Resonance Imaging: MRI

The MRI is a system based on an RF transmitter and an RF receive, which is the target application for ADQ7-FW2DDC.

Scanning Acoustic Microscopy: SAM

Radio frequency based measurements is one natural application area, but also ultrasonic measurement. Even though a SAM transducer has a bandwidth of up to a few 100 MHz, it is an advantage to sample that with several GHz in order to reproduce the transient response with high accuracy. A SAM is a pulse data system, but the pulses are limited in the frequency domain. The frequency band is in fact limited due to the power ramp curve of the transducer pulse. Thus a DDC of ADQ7-FW2DDC can be used to reduce the data rate to the host PC.

Quantum technology

The reading of quantum objects is based on RF receivers, for which the ADQ7-FW2DDC is suitable.

6.8 Beam control Low Level RF

The beam control system of a particle accelerator includes measurement of a set of frequencies at a few GHz. Common frequencies are 1.3 GHz, 1.7 GHz and 2.4 GHz which fall within the preferred region of operation for ADQ7-FW2DDC. The signals can be sampled directly through the wide band analog front-end. No analog mixers are required.

The down conversion can be done in the FPGA, which shortens the loop time, a critical parameter in the control system.

The triggered streaming operation can be used for measuring at the bunches and directly transfer the data to the PC. Allow one trigger per bunch and a high duty cycle. The DDC structure will reduce the data rate to enable streaming to host PC:

7 References

- [1] 19-2226 ADQ7WB datasheet
- [2] 17-2017 ADQ7DC datasheet
- [3] 19-2233 ADQ7WB manual
- [4] 16-1796 ADQ7DC manual
- [5] 19-2325 ADQ7-FW2DDC datasheet
- [6] 19-2335 ADQ7-FW2DDC user guide

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