Synchronizing several ADQ14

ADQ14 is a leading 14-bit digitizer featuring up to 4 channels sampling at up to 2 GSPS each. This application note illustrates how to synchronize several ADQ14 to a multi-channel system.

- Phase-locked clock reference
- Synchronous trigger
- Asynchronous trigger
- Time-stamp
1 Unlimited channel count

The market leading 14 bits digitizer ADQ14 is available in 2 channels at 2 GSPS or 4 channels at 1 GSPS each. This application note shows how to expand a system into very many channels. The topic of synchronization has very many solutions for a large variety of situations. A set of different possibilities are presented here. Select the most suitable for the actual system.

Note that this application note focus on synchronizing several ADQ14 to each other. This is a different topic than to synchronize one ADQ14 to an external equipment.

2 Key elements in synchronization

2.1 Overview

The trigger and the clock are external signals that build up the timing of the system. The clock signal sets the rate of which things happen and the trigger tell when things start. Synchronization of several digitizers then rely on three key elements:

1. The clock frequency has to be aligned and in phase for all ADQ14 units. This requires a shared external clock reference.

2. There has to be a signal that determines the starting point for recording data in each ADQ14. This is done with the trigger signal, which has to be aligned for all units.

3. The time-stamp counts the time in each ADQ14. These counters has to operate in phase in all units.

2.2 Clock reference signal

The clock reference signal on the front panel enables a common external clock reference at 10 MHz. PXIe and MTCA units also support clock reference distribution in the backplane. This common clock reference guarantees the long term stability of the synchronization. Figure 1 (a) illustrate the drift between 2 different digitizers if the clock is not phase locked\(^1\). Figure 1 (b) illustrate phase lock with a common clock reference.

![Figure 1: Effect of common clock reference.](image)

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There are three situations when the synchronization of the clocks are critical:

1. Data driven acquisition on individual channels where the time-stamp is used for measuring the absolute time of individual pulses and do comparison between channels. (This is the typical use case when using firmware option –FWPD.)
2. Recording of very long records. (for example, 1 ppm deviation in clock frequency means one sample deviation in the end of a record of length $10^6$.)
3. Continuous streaming of multiple boards to PC. If not phase locked, the data rate will differ.

There are also situations where the clock reference is not critical.

1. Several cards are triggered in the external trigger from the same source and the records are short.
2. The absolute timing of a data is not critical.

2.3 Trigger

The trigger represents a starting point for the measurements. The trigger is also a real-time reference event in the system. From a synchronization point of view, there are two types of triggers;

1. Synchronous trigger, where the trigger signal is phase locked to the clock reference. The system is then fully synchronous and completely repetitive. Phase locking the trigger to the clock sets the properties of the trigger to be similar to a digital serial link. Key parameters are then set-up and hold time, that is, the time of arrival with respect to the clock edge.
2. Asynchronous trigger, where the trigger signal is not phase locked to the clock reference. There are situations where a non-phase locked trigger can be an advantage. This is for repetitive measurements where the correlation between the trigger and the clock may disturb statistical properties.

2.4 Time-stamp

The time-stamp is the real-time measurement that carry the information from the trigger and clock. The time-stamp counter counts the number of sample periods before a trigger event.

The time-stamp is running with a pace that is related to the actual clock reference. If an external clock reference is used, the time-stamp will also be related to that clock source. In this way it can be considered a real-time clock.

If the ADQ14 is free running, the time-stamp real-time value has the precision of the internal clock. If several digitizers are phase locked with a common clock reference, the time-stamp counters are also in phase, Figure 2.

The time-stamp is a 64 bit integer where the LSB represent ideally 125 ps. The sub-sample precision contains additional information for the external trigger input. All other trigger modes are only resolved on a per sample basis. See the ADQ14 manual (15-1593) for details on how to use the time-stamp.

1. The timing resolution of the external trigger is ideally 125 ps. This means that the sample rate of the external trigger signal is 8 GSPS. The time resolution may differ if there is a deviation in frequency of the clock reference. For example, a 0.1% deviation on the clock reference would give time step of 125.1 ps.
3 Clock reference

3.1 Overview

The clock distribution is the straightforward part of synchronization. It consists of two parts; frequency and phase alignment of several digitizers.

3.2 Clock frequency

A signal from a common source is split and routed to all units. This will guarantee that the frequency, that is, the time base, is common for all digitizers in the system.

3.3 Clock phase

The sampling instant is determined by the phase of the clock signal relative to the analog input signal. From a synchronization perspective, time delay on the clock signal is equivalent to a delay on the analog signal. It is thus equally important to match the cable length for of analog input as for the clock signal. Absolute accuracy cannot be guaranteed without a calibration procedure of the entire system. However, most situations do not require absolute accuracy.

In addition to the potential fixed delay, there is jitter in the internal clock generation. One digitizer has approximately 300 fs RMS jitter. This means that the timing jitter between any pair of ADQ14 digitizers is 300 fs x SQRT(2) = 424 fs (assuming a Gaussian distribution).

3.4 Clock distribution for front panel connection

The clock distribution is a 50 Ohm system.

For only two cards, it is possible to use the clock reference output from one digitizer and connect it to the clock reference input of another digitizer. The two digitizers will then be in phase.

If very many digitizers are used, a fan-out buffer on the clock distribution is required.

3.5 Clock distribution for backplane

The –PXLe and –MTCA form factors support clock reference distribution in the backplane.
4 Trigger properties

4.1 Trigger jitter definition

The trigger jitter consists of two different types, Figure 3.

First; at the trigger input is a Gaussian distributed jitter which affects the timing of the incoming trigger signal edge. This is caused by noise in the analog components of the trigger input stage. The RMS value of this jitter is 10 ps.

The second source is the process of sampling the trigger. The difference between the incoming physical trigger signal and the digital representation of the trigger is a stochastic variable with a rectangular distribution. The RMS value of such a process is \( \text{PERIOD} / \sqrt{12} \). The external trigger is sampled with the 8 GSPS trigger clock, which result in a jitter of 36 ps RMS.

![Figure 3: Sources of jitter on the trigger signal.](image)

4.2 Synchronous trigger set-up and hold time

When the trigger is phase-locked to the clock reference the is timing is comparable to a digital signal with a set-up and a hold time. This section will analyze the synchronous trigger properties.

When using a synchronous trigger, the entire measurement set-up is assumed to be phase-locked. Then the lowest time resolution is the sample rate. The extra sub-sample resolution of the external trigger contains no additional information. However, the sub-sample precision can be used for determine the phase of the trigger signal to analyze the properties of the measurement set-up.

The fastest sample clock is 2 GHz, which means that the timing window is 500 ps. With an RMS jitter of 10 ps, Section 4.1, the set-up and hold times can be set to 6\( \sigma \) which is 60 ps. The eye opening is the 500-60-60 = 380 ps. This timing precision is possible to achieve with accurate systems design. (Note that 380 ps is the signal propagation time in approximately 76 mm coaxial cable.)

When building a synchronous system, the requirements are strict for absolute stability. To simplify the design, the time-stamp is available to resolve uncertainties about the trigger time, Section 4.5.

4.3 About phase locking the trigger

This section adds some comments on phase locking the trigger signal.

The trigger signal is phase locked to the clock reference of the digitizer in the trigger source. There are some key details to achieve this:

- The trigger source needs access to the 10 MHz clock reference of the digitizer. Either, the ADQ14 outputs its internal clock reference and sends it to the trigger source or the trigger source has a clock reference which is sent to the digitizer.
• The trigger source can be the digitizer. Turn on the internal trigger and set the trigger connector to output. The trigger is then phase locked to the digitizer.

4.4 Trigger cable length

The cable length of the trigger signal is critical. The typical propagation properties of a coaxial cable is 66% of the speed of light. This means that trigger resolution of 8 GHz (125 ps) correspond to 25 mm cable length.

4.5 Resolving external trigger with time-stamp

Relaxing the phase requirement of the trigger may simplify the installation greatly. Instead of absolute accuracy of the phase alignment between trigger signal and clock, the time-stamp can be used for resolving the timing of individual channels. Figure 4 illustrates the timing of an external trigger with respect to the sampling of the analog input signal. In the example, the external trigger differs one period of the trigger clock (125 ps) and the first sample differs one period on the sampling clock (1ns). The \textit{TIME\_STAMP} and \textit{RECORD\_START} parameters will tell when the record started and how to align records from several digitizers.

![Figure 4: Phases of external trigger, example.](image)

4.6 Asynchronous trigger

If the trigger signal is not phase-locked to the reference clock it is called asynchronous. This trigger does not have a well determined relation to the sampling clock and will appear at various positions in time according to a rectangular distribution, Figure 3. The trigger jitter is then determined by the resolution of which the trigger is sampled, that is 8 GSPS and the trigger jitter is 36 ps RMS.
5 Distributing external trigger

5.1 Star trigger distribution

The trigger can be distributed in a star configuration in many ways. This section contains examples for various situations. Good impedance matching is essential for suppressing reflections in the system. The ADQ14 is designed for 50 Ohms impedance and standard components for building 50 Ohm systems are generally good enough for trigger distribution.

5.2 Passive splitter

A passive splitter is the most cost-effective solution for a small number of digitizers, Figure 5. Since the trigger signal contains a DC component, a passive splitter has to be DC coupled. This means that the splitter is resistive and the loss is as high as 6dB in each stage. 6 dB means that half the amplitude is lost. To trigger two digitizers is straight forward. Triggering four digitizers will require about 3 to 4 V source drive.

Figure 5: Star trigger distribution with passive splitter.
5.3 Active splitter

An active splitter contains a signal amplifier for each output, Figure 6. Thus there is basically no limit on the number of digitizers that may be triggered with this solution.

The ADQTDU is a trigger fan-out buffer which can be used for trigger distribution. An ADQTDU has 6 outputs and can thus drive up to 24 channels.

It is also possible to use a third party power splitter.

Figure 6: Star trigger distribution with active splitter, for example an ADQTDU.
5.4 **Bussed connection**

The trigger input can be set to high impedance to enable a bussed connection, *Figure 7*. Then one board can trigger several cards. Note that this is not a correct 50 Ohms system and will suffer from reflections. By keeping the cables short, the reflections can be kept under control. It is important to terminate the end point to 50 Ohms in the last digitizer.

This method can be used within a chassis between neighboring cards.

In *Figure 7* (a), the trigger source is an external equipment.

In *Figure 7* (b), one of the digitizers is used as a trigger source. This can be combined with the internal trigger generator for a self contained system. The internal trigger generator is described in the 15-1593 ADQ14 Manual.

*Figure 7: Trigger signal distribution using high impedance setting.*
5.5 Broadcasting a software trigger

A software trigger from the command line is sent to one digitizer at the time. There is no mechanism to
determine when a digitizer will execute a software command.

It is, however, possible to use trigger output in Figure 7 (b) to broadcast a software trigger command
from one digitizer to many others. The trigger output connector may also be used as a GPIO signal. By
using the GPIO functions, and set up the trigger to listen to external trigger, a pulse can be distributed
to all cards simultaneously with only a single WriteGPIO command.

The unit in Figure 8 then acts as the internal trigger source of Figure 7 (b).

### Table

<table>
<thead>
<tr>
<th>#</th>
<th>DESCRIPTION</th>
<th>USER COMMAND</th>
<th>REF</th>
</tr>
</thead>
<tbody>
<tr>
<td>a</td>
<td>Trigger as GPIO</td>
<td>WriteGPIO</td>
<td></td>
</tr>
<tr>
<td>b</td>
<td>Set GPIO direction to output</td>
<td>SetDirectionGPIO</td>
<td></td>
</tr>
<tr>
<td>c</td>
<td>The trigger output and the external trigger input are electrically connected inside the ADQ14</td>
<td></td>
<td></td>
</tr>
<tr>
<td>d</td>
<td>Select external trigger as trigger source. This means that the digitizer will listen the external trigger connector.</td>
<td>SetTriggerMode</td>
<td></td>
</tr>
<tr>
<td>e</td>
<td>Acquisition engine create a record from streaming data.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Figure 8: Broadcast software trigger using Trigger output as GPIO.
5.5.1 Distributing level trigger

Multiple boards may be triggered by level trigger on one channel, Figure 9. This mode is intended for systems with a reference event on one channel that starts the acquisition.

The trigger distribution in Figure 7 (b) may also be combined with this feature.

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**Figure 9: Distributing level trigger.**

<table>
<thead>
<tr>
<th>#</th>
<th>DESCRIPTION</th>
<th>USER COMMAND</th>
<th>REF</th>
</tr>
</thead>
<tbody>
<tr>
<td>a</td>
<td>Select a channel as level trigger</td>
<td>SetupLevelTrigger</td>
<td></td>
</tr>
<tr>
<td>b</td>
<td>Select level trigger as trigger out</td>
<td>SetConfigurationTrig</td>
<td></td>
</tr>
<tr>
<td>c</td>
<td>Internal hardware connection trigger out to trigger in (shared SMA connector)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>d</td>
<td>Select external trigger for triggering</td>
<td>SetTriggerMode</td>
<td></td>
</tr>
<tr>
<td>e</td>
<td>External cable connection to other ADQ14 devices</td>
<td></td>
<td></td>
</tr>
<tr>
<td>f</td>
<td>Select external trigger for triggering</td>
<td>SetTriggerMode</td>
<td></td>
</tr>
</tbody>
</table>

5.6 PXIe backplane star trigger

Using the PXIestar triggers in the backplane requires a PXIe compliant backplane in the chassis and also a trigger-timing module in the trigger-timing slot of the chassis.

This trigger distribution method is not described in this document.
6 Software for multiple boards

6.1 Multiple threads
It is important to notice that the API is not thread safe. It is anyway recommended to implement a multi-threaded application. The key is to make sure that only one thread at the time accesses the digitizer.

6.2 Start-up in a multi-thread software
The start-up procedure for a multi-thread system is
Use ListDevices to find available boards. Do NOT use FindDevices, since it will open communication with the board from the main thread.

The ListDevices returns an ID for each available ADQ14. Start one thread per ID.

System
• 8 Channels
• 1 GSPS
• PCIe form factor
• External asynchronous trigger

Hardware set-up
• ADQ14-4C has 1 GSPS and 4 channels per board. Use two pcs of ADQ14-4C-PCIe.
• Place two digitizers in a PC.
• Use a passive splitter to split the trigger to two cards, see Section 5.2. An alternative is a bussed connection, see Section 5.4.
• Use clock reference output on one of the cards and connect to clock reference input of the other card, see Section 3.4.

Software set-up
• Use time-stamp reset to synchronize timing between the cards (15-1593-PA15 ADQ14 Manual section 5.1.4)
• Use trigger blocker to arm the systems to start all cards simultaneously (15-1593-PA15 ADQ14 Manual section 5.1.5)
7.2 Building a large system (up to 96 channels), Figure 11

**System**
- 96 Channels
- 1 GSPS
- PXIe form factor

**Hardware set-up**
- ADQ14-4C has 1 GSPS and 4 channels per board. Use 24 pcs of ADQ14-4C-PXIe.
- Place 4 digitizers in a medium-sized chassis (6 chassis in total)¹.
- Connect triggers with bussed connection in groups of 4 digitizers. This means 6 groups. See Section 5.4.
- Use an ADQTDU² to distribute a trigger to all the 6 groups. See Section 5.3.
- Use the backplane distribution of the clock reference.
- Use an ADQTDU² to distribute a clock reference to all the chassis.
- Optional: Use ADQ10GBE to get a fast Ethernet connection for sending data between the chassis.

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¹. It is also possible to use three large chassis with 8 digitizers in each, but then Linux OS is required. The computing power is also a parameter since there is one controller per chassis; fewer chassis means less computing power.

². It is also possible to use a third party fan-out buffer; active or passive.

³. It is also possible to use a third party fan-out buffer; active or passive.
chassis. The ADQ10Gbe can be connected as indicated and send data to its neighbors or via a switch to any other chassis.

**Software set-up**

- Use time-stamp reset to synchronize timing between the cards (15-1593-PA15 ADQ14 Manual section 5.1.4)
- Use trigger blocker to arm the systems to start all cards simultaneously (15-1593-PA15 ADQ14 Manual section 5.1.5)
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