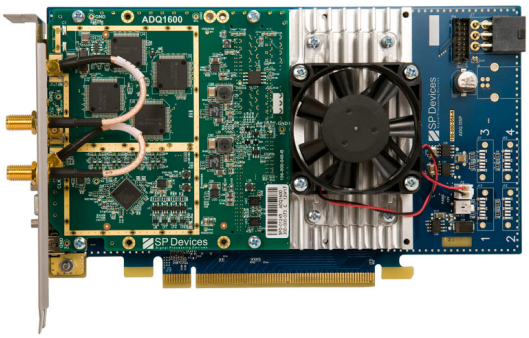


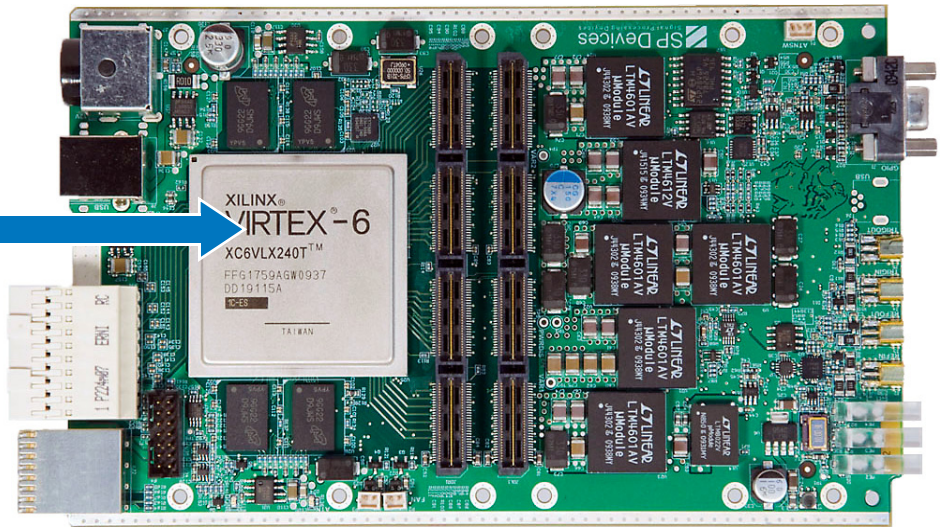
ADQ Development Kit

ADQ Development Kit is a tool for developing custom firmware in the FPGA of an ADQ series digitizer. SP Devices' digitizers are characterized by a combination of high speed and high resolution. The amount of data from the digitizer is thus very high. The most efficient way of processing the data is through a real time implementation inside the FPGA on the digitizer. The ADQ Development Kit opens the FPGA for implementation of real-time signal processing algorithms.

SP Devices' FPGA development project

Example code for real-time signal processing

Custom real-time solutions



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Principle

The principle structure of the ADQ Development Kit is shown in **Figure 1**. The ADQ Development Kit is a design project for the Xilinx ISE tool. The project contains a Framework netlist (NGC) file with necessary digitizer infrastructure and a User Logic area for custom real time functions. The Framework NGC contains, for example, ADC interface, DRAM controller and programmable signal processing. It also contains predefined signal processing that can be configured or removed in the custom design. The removable blocks are available in the standard digitizer product, but they may occupy a significant amount of resources inside the FPGA. If the custom design do not require these blocks, they may be removed to free resources.

The User Logic area has a set of data buses in and out and control signals in and out. There is also example source code[1]. The software application can communicate with custom firmware in User Logic through a set of registers.

The procedure of working with the development kit is

- Include/exclude specific blocks (box in **Figure 1**)
- Select data flow connections in User Logic (wide arrows in **Figure 1**)
- Select control signals in User Logic (narrow arrows in **Figure 1**)
- Implement custom firmware in User Logic
- Implement custom software functions to control the User Logic.

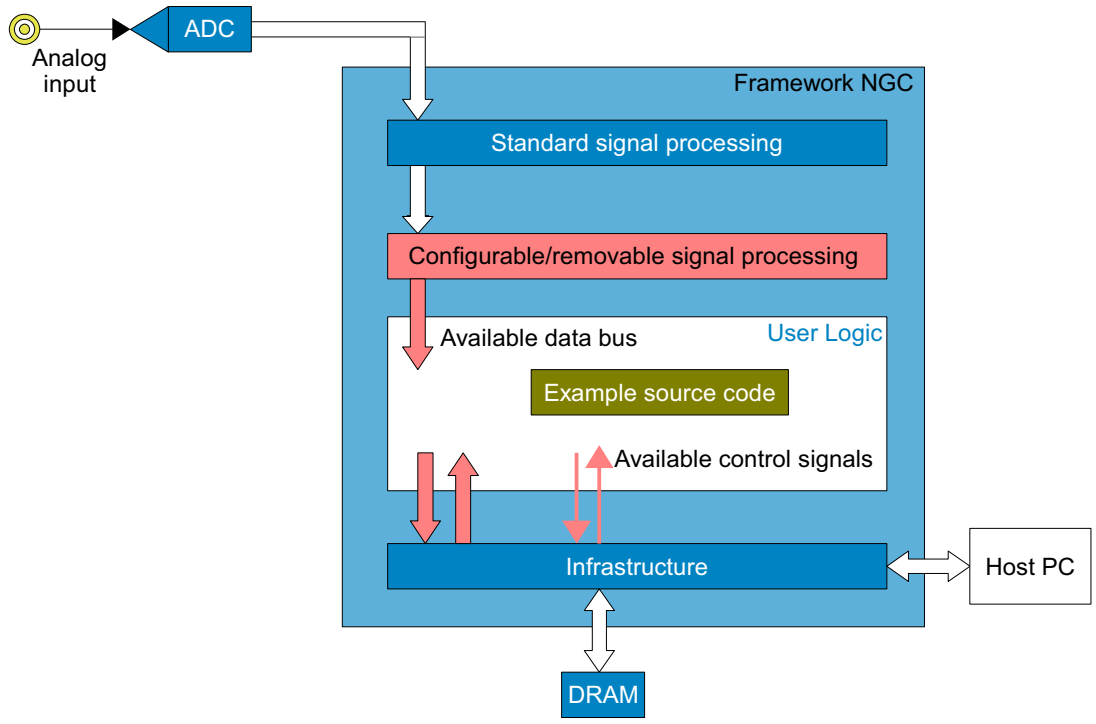

Figure 1: Principle of the ADQ Development Kit.

1. The examples differ between different digitizer models.

ADQ Development Kit in ADQ V6

A detailed view of the ADQ Development Kit is given in **Figure 2** and the blocks are described in **Table 2**. For better understanding, some nodes are indexed and listed in **Table 1**.

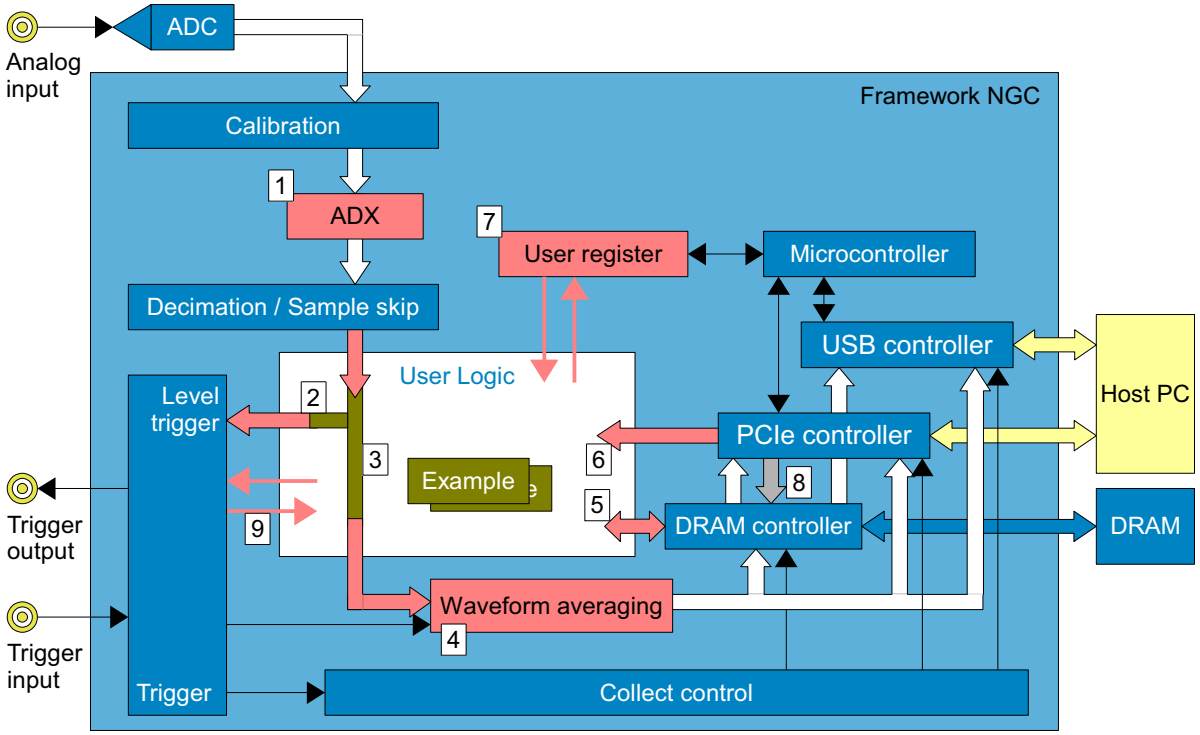

Figure 2: Detailed view of ADQ Development Kit in the ADQ V6 digitizer.

#	FUNCTION	CUSTOM USE CASE EXAMPLE	REF
1	SP Devices' proprietary interleaving IP ADX is available on interleaved digitizers.		[2]
2	The level trigger function can be used for triggering on result from custom calculations.	Power calculation, trigger at a certain power level.	[1]
3	Save raw data or custom data.	Use a power level trigger, but record raw data. Do custom calculations of signal properties and record that.	[6]
4	Waveform averaging and triggered streaming FIFO.		[3]
5	Data from DRAM into user logic (ADQ412 only).	Send data over 10GbE link in ADQ412-MTCA.	[6]
6	Send data from the PCIe bus into user logic. (ADQ412 only)	Send data between units for processing of combined channels.	[6]
7	User registers to control the user logic. The use of the registers is defined by the user.	Filter coefficients in a configurable filter. Read out calculation results with low update rate, such as mean power.	[6]
8	Write data to DRAM from PCIe interface. (Used in SDR14 only for downloading AWG segments.)		[8]
9	Internal signals in the trigger block.	Use internal trigger for timing of custom operations. Create custom triggers.	[1]

Table 1: Key signal nodes in ADQ Development Kit. See Figure 2.

	BLOCK	DESCRIPTION	REF
	Calibration	DC-calibration of gain and offset. Both factory calibration and user calibration are available.	[5]
	ADX	SP Devices' proprietary technology for interleaving of ADCs.	[2]
	Decimation/sample skip	This is a standard function in the Framework NGC. A sample skip is a procedure to reduce the data rate inside the FPGA by discarding samples. The data rate is adjusted before going into User Logic.	[5]
	User Logic	This is the area where custom code is placed. There are several connections of different types; data and control.	[6]
	Waveform averaging	This is a FIFO holding the accumulator of the waveform averaging. The FIFO is also used for triggered streaming.	[3] [10]
	Trigger	The trigger unit handles all the trigger events. A set of control signals from the trigger module is available in the User Logic for interaction with the built-in acquisition control.	[1]
	Collect control	Internal function that controls acquisition and controls the flow of data in the digitizer.	
	DRAM controller	The DRAM controller handles the on-board DRAM.	[6]
	PCIe controller	This is the PCIe controller for the data link to the host computer. Form factors, PCIe, cPCIe/PXIe and Micro-TCA use the electrical signaling defined by PCIe.	[6]
	USB controller	This is the USB controller for the data link to the host computer. This is the data link in digitizers in the USB form factor.	[6]
	Microcontroller	The microcontroller is an internal block that handles user commands.	
	User register	This is a register file available in the User Logic. It is a link between the software application and the custom FPGA functions in User Logic.	[6]

Table 2: Blocks in ADQ Development Kit. See Figure 2.

Available resources

Different digitizer models require different amount of FPGA resources. **Table 3** lists available resources for the different models. **Table 3** also lists configuration options. There may be deviations between different revisions of the ADQ Development Kit. Presented figures are from 2013-09-20

MODEL	REGISTERS	LUTS	DSP48E1	BRAM [MBIT]	INCLUDED BLOCKS	
					WFA	ADX
Total in FPGA[1]	301 000	241 000	768	15	-	-
ADQ108	82%	72%	88%	83%	-	-
ADQ412-3G[2]	68%	56%	52%	26%	WFA	2 x ADX2
ADQ412-3G[3]	77%	69%	96%	47%	WFA	-
ADQ412-3G[3]	77%	69%	96%	73%	-	-
SDR14	83%	74%	81%	37%	-	2 x ADX2
ADQ1600	82%	75%	76%	31%	WFA	ADX4
ADQ1600	82%	75%	76%	71%	-	ADX4

Table 3: Available resources

1. Xilinx Virtex6 XCV6LX240T
2. Availability of ADQ412 Development Kit with ADX has to be confirmed.
3. 4-channels mode

Accessing the User Logic from the ADQAPI

The control of the functions in User Logic is done via the User Registers. Use the ADQAPI commands ReadUserReg() and WriteUserRegister() to access the registers. There are 16 pre-defined registers. The data channels in and out of User Logic can in principle be used for any type of information (not only ADC data). Control information may be packeted as data and sent via these interfaces.

Including/excluding ADX

SP Devices' interleaving technology ADX is only available on interleaved digitizers. The ADQ412 can operate both in interleaved 2 channel mode and in non-interleaved 4-channel mode. In ADQ412 running in 4-channel mode, the ADX is not used. It is thus possible to exclude that block to save resources in the FPGA.

Including/excluding waveform averaging

Waveform averaging is optimized for maximum length of the waveform (record). Most of the Block RAMs in the FPGA are thus consumed by the WFA. It is possible to exclude WFA and use the Block RAM for custom functions.

GPIO

Instandard firmware, the GPIOs are accessed from registers in the micro controller. With the ADQ Development Kit it is possible to incorporate the GPIO in real time data and control flow.

The GPIO signal is buffered from the input pin on the FPGA, and then routed directly to the user logic, without being clocked. This means that it can be sampled on any of the clocks routed to the user logic core:

Micro controller clock (50 MHz). This is a free running fixed clock. Using this clock makes GPIO synchronized to the Micro controller.

Data Clock. The data clock is a function of the sampling frequency and the GPIO is then phase locked to data. This frequency is depending on digitizer model but is typically near 200MHz.

2 X Data clock. The data clock is a function of the sampling frequency and the GPIO is then phase locked to data. This frequency is depending on digitizer model but is typically near 400MHz.

A further option is to parallelize the signal using an ISERDES block (serial to parallel converter). That way higher timing precision can be achieved. The ISERDES block also has protection against meta-stability.

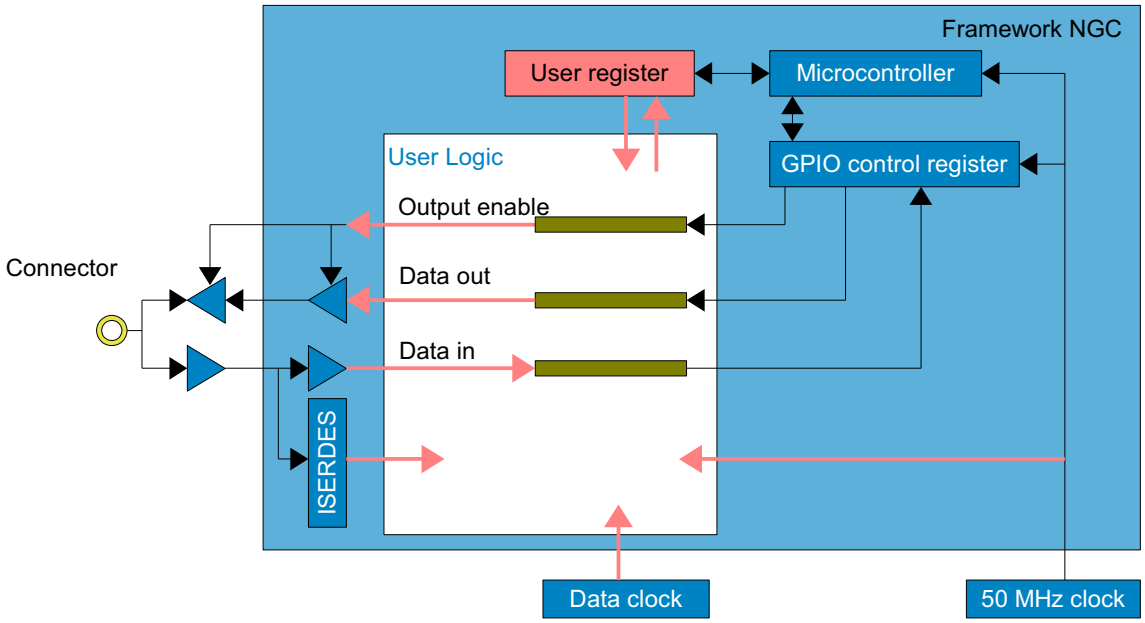

Figure 3: ADQ V6 GPIO

Example source code

The ADQ Development Kit contains a set of source code examples. The examples differ between the digitizer models, see **Table 4**.

All models has a by-pass connection, that connects the data wires to build a standard digitizer.

All models also has an 8 taps FIR filter for illustration of using the ADQ Development Kit. The coefficients are written into the User Registers 0 to 7.

MODEL	EXAMPLES	REF
ADQ108	By-pass connection	[6]
	FIR filter	[6]
ADQ412	By-pass connection	[6]
	FIR filter	[6]
ADQ412-3G	By-pass connection	[6]
	FIR filter	[6]
ADQ412-4G	By-pass connection	[6]
	FIR filter	[6]
SDR14	By-pass connection	[6]
	Loop back	[4]
	Radio	[7]
	FIR filter	[6]
ADQ1600	By-pass connection	[6]
	FFT	[9]
	FIR filter	[6]

Table 4: Source code examples in the ADQ Development Kit

References

[1] 11-0701-B-Trigger_ApplicatioNote.pdf
[2] 13-0962-ADX_IP_user_guide_for_ADQ_A.pdf
[3] 11-0699-PB5-ApplicationNote_WFA.pdf
[4] 12-0894-A_Loopback_ApplicationNote_SDR14.pdf
[5] 08-0214_ADQ-API_ug.pdf
[6] 11-0612_UsersGuide_ADQ_V6_DevKit.pdf
[7] SDR14_transceiver_mastersthesis.pdf
[8] 12-0826-C-ApplicationNote_AWG
[9] Master Thesis Report FFT.pdf
[10] 13-0937-A-Data_transfer_ApplicatioNote.pdf

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