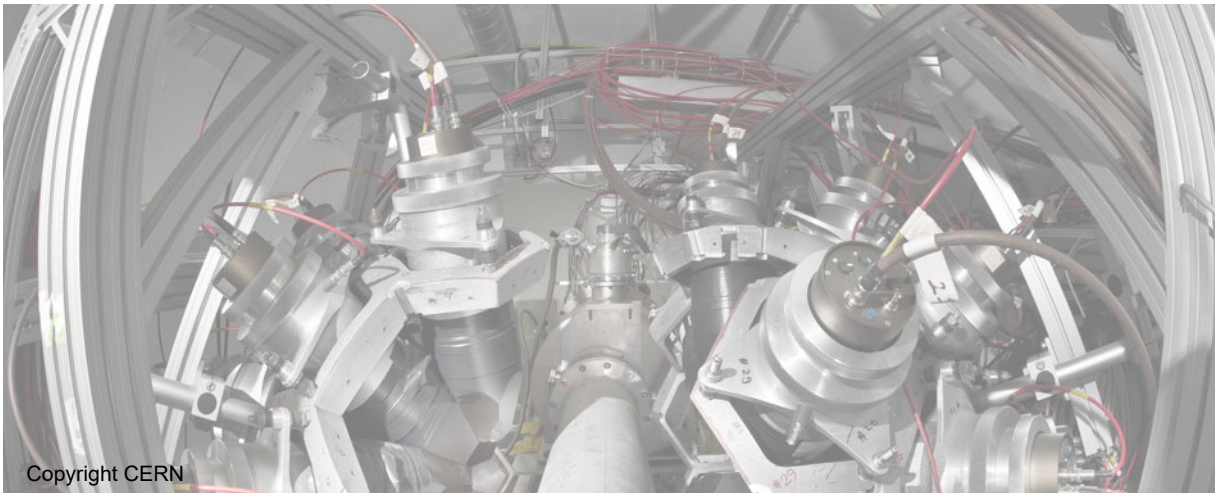
ADQ12DC Datasheet

ADQ12DC is a high-performance 12-bit data acquisition board which offer complete and versatile solutions for advanced measurements. It comes with a generous set of firmware, and software features which help simplify integration. Every aspect of the measurement process from the detector, real-time signal processing, data visualization, and more are included. Selected features include:

- *Flexible choice of channel count and multi-board synchronization*
- *Advanced analog front-end supporting high input bandwidth*
- *Open FPGA for real-time DSP and stand-alone application-specific firmware*
- *Up to 3.2 GByte/s data transfer rate the host PC*
- *A selection of application-specific firmware for efficient system integration*



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ADQ12DC Datasheet

Features

- 2 or 4 analog channels (options)
- 1 GSPS sampling rate per channel
- 12 bits vertical resolution
- DC-coupled with 700 MHz analog BW
- Programmable DC-offset
- Internal and external clock reference
- Internal and external clock generator
- Clock reference output
- Internal and external trigger
- Trigger input / output connector
- Multi-channel synchronization
- Timestamp for real-time operation
- 2 GByte data memory
- Up to 3.2 GBytes/s data transfer to PC
- Data interface PCIe Gen2 x8

ADQ12 Development Kit

- Open FPGA for custom applications
- Real-time signal processing

Applications

- RADAR
- LIDAR
- Wireless communication
- High-speed data recording
- Test and measurement
- Ultrasonic ranging
- Time-of-flight scientific instruments
- Swept-Source OCT
- Thomson scattering

Advantages

- Fast PCIe Gen2 x8 interface for compact systems integration.
- Analog front-end that support a wide range of detectors and allows for re-use and streamlined cost-efficient maintenance.
- Real-time FPGA custom processing enables compact system design.
- SP Devices' design service is available for fast integration to reduce time-to-market.

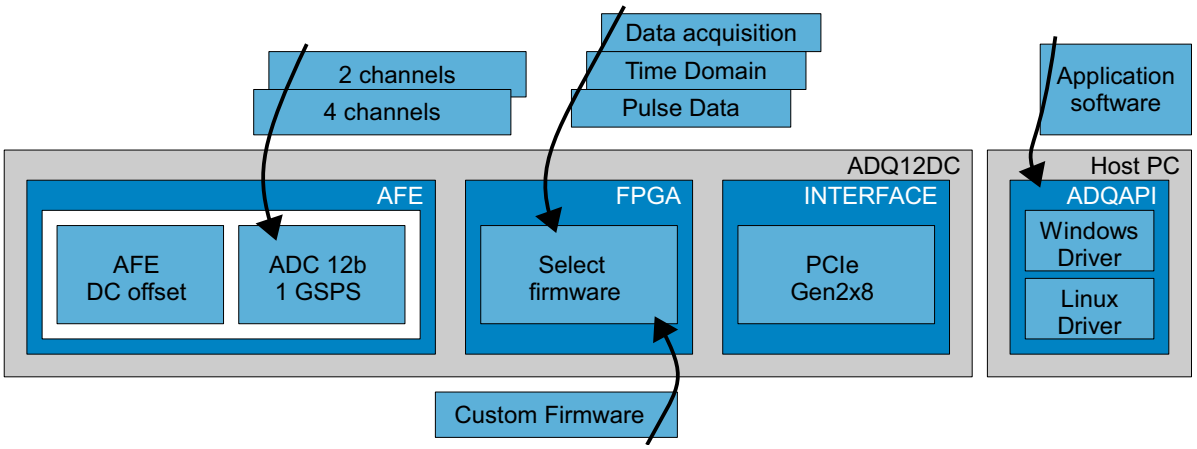
Flexible digitizer solution for the complete signal chain

ADQ12DC supports the entire signal chain, from the detector to the application integration.

The wideband high dynamic range analog front-end offers options for a variety of advanced detectors.

Due to the vast amounts of data produced the signal processing support is key. Therefore ADQ12DC includes several layers of high-speed signal processing; the open FPGA and application-specific firmware enables integration of real-time algorithms and very compact system design; the software development kit for application integration is available both for Windows and Linux.

The high-speed Gen2 x8 enables efficient communication between the firmware and the software.



1 Selection guide

There are several options for ADQ12DC. This guide will help you to select the right options. Follow the procedure listed to find the best product for your application. Each of the items in the list are described further in this document. The table below to shows which combinations that are available.

1. Select the number of channels; –2C, or –4C.
2. Host interface form factor single-slot PCIe; –SSPCIE.
3. Select one or several of the firmware packages; –FWDAQ, –FWATD, –FWPD.
4. Add ADQ12 Development Kit for custom real-time signal processing in the FPGA.

OPTION		ADQ12DC –2C	ADQ12DC –4C
Key parameters (Factory installed)			
Number of channels		2	4
Firmware (Field upgrade supported)			
ADQ12 Development Kit[1]		✓	✓
Acquisition[2]	–FWDAQ	✓	✓
Advanced time-domain	–FWATD	✓	✓
Pulse data	–FWPD	✓	✓
Host interface form factor (Factory installed)			
PCIe	–SSPCIE	✓	✓

1. The ADQ12 Development Kit is available for –FWDAQ and –FWPD.
2. Included with the ADQ12DC.

Note: The firmware options –FWATD, and –FWPD are a replacement (not an add-on) of the standard –FWDAQ firmware. This means that some of the functions in examples and in documentation for –FWDAQ may not be available. Only the API functions and examples especially designed for the specific firmware option will work when that firmware option is loaded. Please note that with each device you are always entitled to load the standard –FWDAQ onto the device and use the device with the standard firmware acquisition modes.

Note: Changing firmware consists of uploading new contents to the on-board flash memory and restarting the digitizer. The restart requires a cold reboot as the PCIe link has to be re-enumerated by the BIOS of the host system.

2 Technical data

All values are typical unless otherwise noticed.

Table 1: General Parameters

PARAMETERS		ADQ12DC–2C	ADQ12DC–4C
Key parameters			
Channels		2	4
Sample rate / channel	[GSPS]	1	
Resolution	[bits]	12	
Data memory[1]	[GByte]	2	
Power			
Power supply	[V]	12	
Power dissipation	[W]	39	48

1. The data memory is shared between data (2 bytes per sample) and record headers. The memory is shared between all activated channels.

Table 2: Analog input

PARAMETERS		ADQ12DC–2C	ADQ12DC–4C
Analog inputs			
Coupling		DC	
Input Impedance	[Ω]	50	
Input range	[V_{pp}]	0.5	
Bandwidth lower –3 dB	[Hz]	DC	
Bandwidth upper –1 dB	[MHz]	500	
Bandwidth upper –3 dB	[MHz]	700	
Connector		SMA	
Variable DC-offset range[1]	[V]	±0.25	

1. Software controlled setting.

Table 3: Dynamic performance measured for a 71 MHz, –1dBFS single sine wave input

PARAMETERS		ADQ12DC–2C	ADQ12DC–4C
Analog performance with overvoltage protection activated			
SNR	[dB]	57	
SNDR	[dB]	57	
SFDR	[dBc]	70	
ENOB	[bits]	9.2	

Table 4: Clock

PARAMETERS		ADQ12DC–2C	ADQ12DC–4C
Internal Clock Reference			
Frequency	[MHz]	10	
Accuracy	[ppm]	± 3 ± 1/year	
External clock reference input			
Frequency (min – max)	[MHz]	10 MHz ± 5 ppm	
Signal level (min – max)	[Vpp]	0.5 – 3.3	
Impedance AC	[Ω]	50	
Impedance AC (high[1])	[Ω]	200	
Impedance DC	[Ω]	10 k	
Connector		SMA	
Clock reference output			
Frequency	[MHz]	Set by selected clock reference	
Signal level	[Vpp]	1.2 (into 50 Ω load)	
Impedance AC	[Ω]	50	
Impedance DC	[Ω]	10 k	
Duty cycle		50% ± 5%	
Connector		SMA	
External clock source			
Frequency	[GHz]	1	
Signal level into 50 Ω (min – max)	[Vpp]	0.5 – 3.3	

1. Software-controlled high-impedance setting for large fan-out situations.

Table 5: Trigger / GPIO front panel connector

PARAMETERS		ADQ12DC–2C	ADQ12DC–4C
External trigger used as input			
Trigger frequency (max)	[MHz]	1	
Signal level (min – max)	[V]	–0.5 to 3.3	
Threshold[1]	[V]	0 to 3	
Sensitivity	[mVpp]	200	
Time resolution	[ps]	125	
Excess jtter[2]	[ps]	25	
Impedance DC	[Ω]	50	
Impedance DC (high[3])	[Ω]	500	
GPI data rate	[Mbit/s]	125	
Connector		SMA	
External trigger used as output			
PRF (max)	[MHz]	125	
Signal level output low max	[V]	0.1	
Signal level output high min	[V]	1.2 (into 50 Ω load)	
Impedance DC	[Ω]	50	
GPO data rate	[Mbit/s]	125	
Connector		Shared with trigger input	

1. Software-programmable level.
2. The trigger is synchronous to the sampling and can be resolved with sub-sample precision. The excess jitter is jitter added to the trigger signal inside the ADQ12DC.
3. Software-controlled high-impedance setting for large fan-out situations.

Table 6: Sync / GPIO connectors

PARAMETERS		ADQ12DC–2C	ADQ12DC–4C
External sync input			
PRF (max)	[MHz]	1	
Low level input voltage max	[V]	0.8	
High level input voltage min	[V]	2	
Impedance DC	[Ω]	50	
Impedance DC (high[1])	[Ω]	500	
GPI data rate	[Mbit/s]	125	
Connector (–SSPCIE)		MCX (on PCB inside PC cabinet)	
External sync output			
PRF (max)	[MHz]	>1	
Low level output voltage max	[V]	0.1	
High level output voltage min	[V]	1.2 (into 50 Ω load)	
Impedance DC	[Ω]	50	
GPO data rate	[MHz]	125	
Connector (–SSPCIE)		MCX (on PCB inside PC cabinet)	

1. Software-controlled high-impedance setting for large fan-out situations.

Table 7: Environment

PARAMETERS		ADQ12DC–SSPCIE
Data rate		
Communication standard		PCIe Generation 2 by 8 lanes
Data rate sustained [1]	[MBytes/s]	3200
Mechanical		
Weight	[g]	390
Mechanical bus width	[lanes]	16 [2]
Board width	[slot]	1
Board length	[mm]	236
Electrical		
Power supply		6-pin ATX power
Bus width electrical (PCIe Gen2 x8)	[lanes]	8
Temperature range		
Operation	[°C]	0 to 45 [3]
Compliances		
CE		✓
RoHS2		✓
FCC		Exclusion according to CFR 47, part 15, paragraph 15.103(c)

1. This is depending on the capability of the complete system including the host computer.
2. The wide connector is required to support the weight of the board.
3. This is the temperature of the air in to the fan of the ADQ12DC.

Table 8: Firmware options: functions overview

PARAMETERS	–FWDAQ	–FWATD	–FWPD	COMMENT
Signal enhancement IP				
DBS	✓	✓	✓	Digital Baseline Stabilizer
Trigger modes				
Software trigger	✓	✓		
External trigger	✓	✓	✓	
Common level trigger	✓	✓		All channels trigger on one selected channel
Individual level trigger			✓	Each channel triggers independently
Internal trigger	✓	✓		
Trigger output				
Internal trigger	✓	✓	✓	
Trigger event	✓	✓	✓	
Clock				
All clock modes	✓	✓	✓	
Sample skip	✓	✓		
Data acquisition modes				
Continuous streaming	✓			
Triggered streaming with header	✓	✓	✓	
Triggered streaming without header	✓			
Multi-record	✓			

Table 9: Data acquisition parameters for –FWDAQ

PARAMETERS		ADQ12DC–2C	ADQ12DC–4C
Triggered streaming[1]			
Rearm time	[ns]	8	
Pretrigger max	[samples]	16 ki	
Pretrigger step	[samples]	4	
Trigger delay max	[samples]	$2^{32} - 1$	
Trigger delay step	[samples]	4	
Record length max	[samples]	2 Gi	
Record length min	[samples]	8	
Record length step	[samples]	1	
Multi-record[1]			
Re-arm time	[ns]	1000	
Pretrigger max	[samples]	Record length	
Pretrigger step	[samples]	4	
Trigger delay max	[samples]	$2^{32} - 1$	
Trigger delay step	[samples]	4	
Record length max	[samples]	500 Mi	250 Mi
Record length min	[samples]	32	
Record length step	[samples]	4	
Continuous streaming			
Data rate		PC link speed limit	

1. Use Multi-record parameters for pretrigger length larger than 16 kiSamples. If pretrigger is shorter than 16 kiSamples use the Triggered streaming parameters.

Table 10: Software support[1]

PARAMETERS	ADQ12DC–2C	ADQ12DC–4C
Operating systems[2]		
Windows 7, 32-bit and 64-bit	✓	
Windows 8 / 8.1, 32-bit and 64-bit	✓	
Windows 10, 32-bit and 64-bit	✓	
Linux	✓	
Application integration		
ADCaptureLab[3]	Acquisition and analysis	
MATLAB[4]	API, examples	
C/C++	API, examples	
.Net (C#, Visual Basic)	API, examples	
Python	Example scripts	
LabVIEW [5]	Low level functions and example code	

1. Full performance is only guaranteed using supplied examples in C/C++ programming language.
2. See “15-1494 Operating System Support” for supported distributions.
3. Windows only and firmware option –FWDAQ only. Intended for basic measurements. Limited function support.
4. Windows only and firmware option –FWDAQ only.
5. Windows only and firmware option –FWDAQ only.

3 Absolute maximum ratings

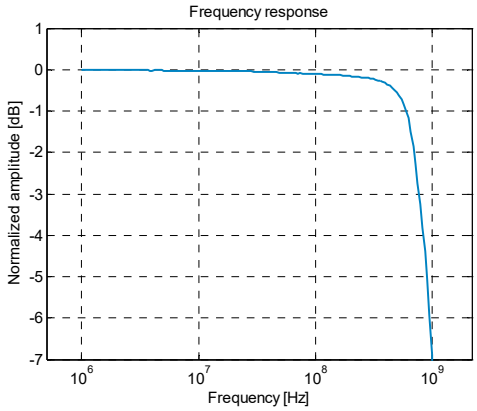
Exposure to conditions exceeding these ratings may reduce lifetime or permanently damage the device. The ADQ12DC has a built-in fan to cool the device. The built-in temperature monitoring unit will protect the ADQ12DC from overheating by temporarily shutting down parts of the device if an overheat situation would occur.

The SMA connectors have an expected life time of 500 operations. For frequent connecting and disconnecting of cables, connector savers are therefore recommended.

Table 11: Absolute Maximum Ratings

PARAMETERS		ADQ12DC–2C	ADQ12DC–4C
Analog input with overvoltage protection			
Signal level to GND	[V]	±4	
External clock reference			
Signal level AC	[Vpp]	5	
Signal level DC	[V]	± 5	
External trigger input			
Signal level to GND (min)	[V]	–2.3	
Signal level to GND (max)	[V]	+5	
External sync input			
Signal level to GND (min)	[V]	–0.5	
Signal level to GND (max)	[V]	+3.8	
Power supply			
Voltage to GND (min)	[V]	–0.4	
Voltage to GND (max)	[V]	14	
Temperature			
Operating (min)	[^{o}C]	0	
Operating (max)	[^{o}C]	45	
Standard GPIO			
Trigger input		See trigger specification **Table 5**	
Sync		See sync specification **Table 6**	

4 Frequency response



Bandwidth (–3 dB)	700 MHz
1 dB flatness	500 MHz

Figure 1: ADQ12DC–4C and ADQ12DC–2C.

5 Spectral performance

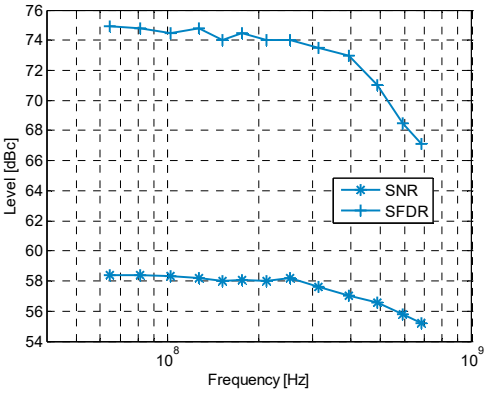


Figure 2: ADQ12DC–4C and ADQ12DC–2C.

6 Frequency domain

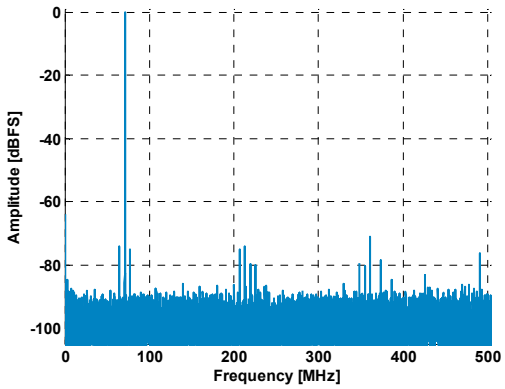


Figure 3: ADQ12DC–4C: 71 MHz.

7 Integrating the ADQ12DC

Figure 4 illustrates how ADQ12DC supports the key parts of the system integration.

7.1 Detecting the analog signal

The analog front-end (AFE) combines high dynamic range with high bandwidth to support the most advanced detectors. The DC-coupled front-end has high sensitivity to simplify the interfacing.

7.2 Timing and synchronization

The clock management and trigger support connects with the infrastructure of the system. The ADQ12DC can act as master and generate timing for the entire system and thereby save additional timing cards. It can also receive trigger and clocks from other devices. Synchronization and GPIO signals allow advanced sequencing.

Synchronization might be needed between ADQ12DC and other types of equipment. This is supported by the clock and trigger signals.

In a multi-channel system, synchronization between several ADQ12DC is needed. The details provided in the application note “15-1583 ADQ14 synchronizing several units” are also applicable to ADQ12DC and shows how to synchronize several ADQ12DC units in a large-scale installation.

7.3 Real-time signal processing

The data acquisition engine in the FPGA supports several methods for acquiring data and transfer it to the host PC. Since the data rate from the ADC is high, some parts of the application is preferably integrated into the FPGA as to relax the load on the CPU in the host computer. There is a set of application-specific firmware options available to enable efficient real-time signal processing. In addition, the FPGA is opened to the user through the ADQ12 Development Kit for integration of custom algorithms.

7.4 System integration

The interface to the host PC is one important parameter in the system integration. To enable an optimal solution, the ADQ12DC offers a high speed PCIe interface. The mechanical properties enable an optimal placement of the ADQ12DC inside the target system PC.

7.5 Building the application

The open software development kit (SDK) is a software package including drivers and API (ADQAPI) for integrating the ADQ12DC into an application. A number of examples and application notes simplify the integration process and shorten the time-to-market.

Partitioning the application between a high-level analysis software in the host PC and a low-level real-time data analysis in the open FPGA enables high performance applications to run on a cost-efficient PC solution.

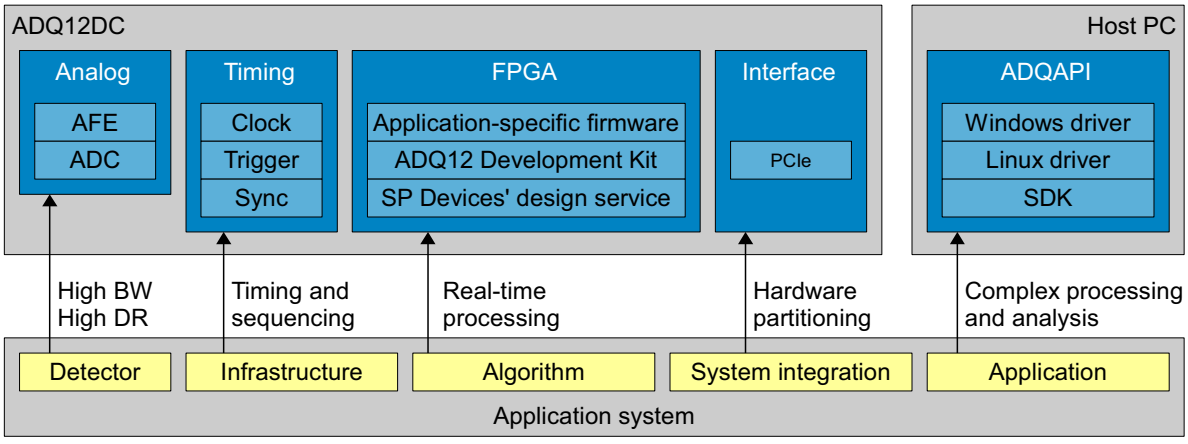


Figure 4: Integrating the ADQ12DC into a system.

8 Software tools

8.1 Operating systems

The software package includes drivers for the most common versions of Windows and several Linux distributions.

8.2 Software Development Kit

The ADQ12DC digitizer is easily integrated into the application by using the software development kit (SDK). The SDK is included free of charge with the ADQ12DC. The SDK includes programming examples and reference projects for several platforms. All functions are described in detail in document “14-1351 ADQAPI Reference Guide”. Please note that the data-rate performance is depending on the selected programming environment. Best result is achieved for the C/C++ interface. The SDK enables rapid custom processing of large amounts of data and real-time control of the digitizer.

8.3 ADCaptureLab GUI for –FWDAQ

The ADQ12DC is supplied with the ADCaptureLab software providing quick and easy control of the digitizer. The tool offers both time-domain and frequency-domain analysis, see **Figure 5**. Data can be saved in different file formats for off-line analysis. With ADCaptureLab, the ADQ12DC operates as a benchtop oscilloscope.

Note: The GUI ADCaptureLab only support a subset of the functionality offered by the ADQ12DC. The full potential of the ADQ12DC is achieved using the SDK. ADCaptureLab is available for Windows only and the firmware option –FWDAQ only.

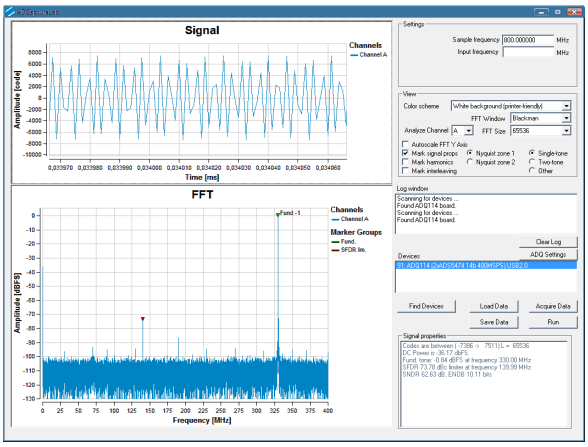


Figure 5: ADCaptureLab typical screen shot.

9 Block diagram

A detailed block diagram ADQ12DC–4C is shown in **Figure 6**. The following sections describe the parts of the ADQ12DC in detail. See also “18-2199 ADQ12DC Manual” for more details on how to operate the ADQ12DC.

This datasheet describes functions included in the standard data acquisition firmware package –FWDAQ. Functionality of optional application-specific firmware packages is described in their respective datasheets (14-1397 and 15-1455).

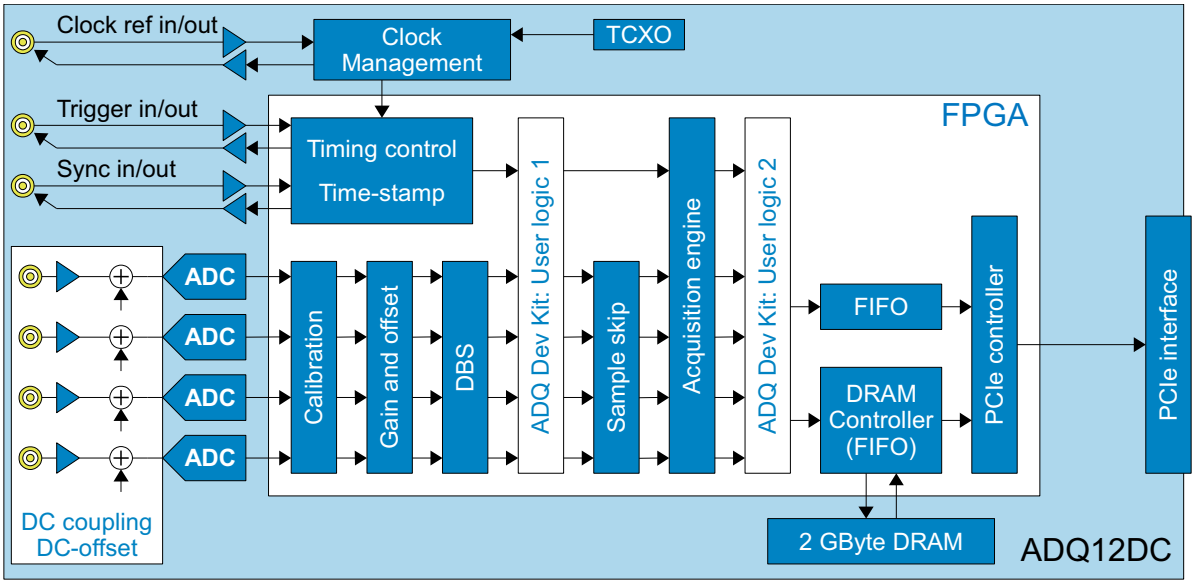
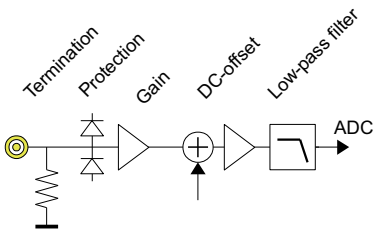


Figure 6: Block diagram for ADQ12DC–4C.

10 Analog front-end options

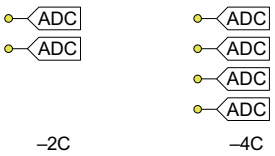


DC-coupling

For pulse data measurements.

The DC-coupled AFE contains overvoltage protection and a software programmable DC-offset. Overvoltage protection is crucial in pulse data systems where high voltage detectors are driving the input. It reduces the risk of damage at accidental discharges.

The DC-coupled AFE also has a noise-suppression through a bandwidth limiting low pass filter at 500 MHz.

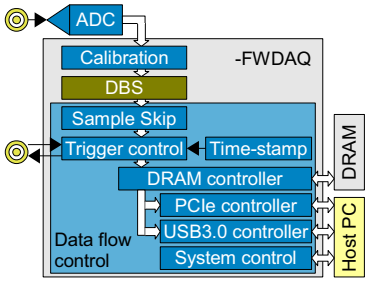


Number of channels (–2C, –4C)

The channel count options are offered to meet various measurement situations.

ADQ12DC is available with 2 or 4 channels depending on the measurement situation. The maximum number of channels is factory installed. The user can select to activate only a sub-set of the installed channels via the software interface.

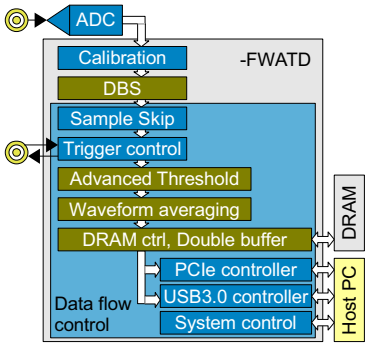
11 Firmware options



Data acquisition firmware (–FWDAQ)

For general purpose high-speed data recording.

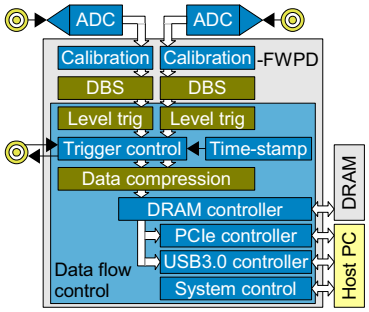
The data acquisition firmware –FWDAQ is the default firmware for ADQ12DC and is always included. Supported data acquisition modes are continuous multi-record, triggered streaming and continuous streaming, **Section 12**. The supported trigger modes are external, internal, software and level trigger, as well as internal and external clock reference, **Section 14** and **15**).



Advanced time-domain (–FWATD)

For time-domain analysis of synchronized repetitive events.

The option –FWATD includes an advanced threshold algorithm for non-linear discrimination of noise. There is also waveform averaging (WFA) for real-time accumulation of repetitive events, that contributes to improved SNR. The WFA can take waveforms up to 1 MSamples in length. The WFA may also be split into several accumulations of a total length up to 1 MSamples to simplify readout scheduling. A stable baseline is achieved by the DSB, **Section 19**.

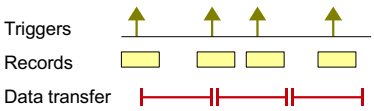


Pulse data (–FWPD)

For capturing random events.

With –FWPD, each channel can be individually event-triggered to capture random events. The trigger levels are user-defined levels or filtered data for adaptive thresholding. To support random event lengths, the record lengths are dynamic. Data compression through zero suppression saves disk space.Thanks to the DRAM, bursts of events can be buffered before transferring data to the host PC, **Section 12**. A stable baseline is achieved by the DSB, **Section 19**.

12 Data recording

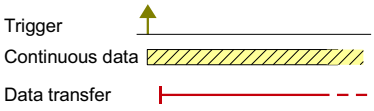


Triggered streaming

Use triggered streaming for maximum throughput.

At each trigger, a record (a set of continuous data) is captured. The record is buffered in the DRAM, which act as a FIFO, and transferred to the host PC. This large 2 GByte FIFO enables bursts of triggers at very high rate. The large FIFO also guarantee reliable high-speed transfer to the PC.

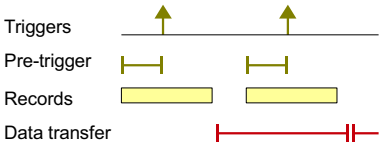
Each record has a header with timestamp and identifiers for post-processing analysis of the data.



Continuous streaming

Continuous recording of very long events.

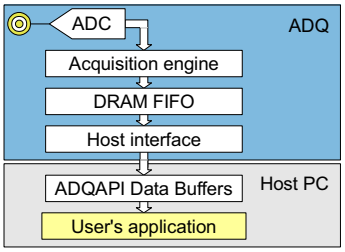
The recording is started by a trigger event and continue until it is terminated by the user. The continuous streaming mode produce a large amount of data and is often combined with a data reduction method in the FPGA. This is, for example, channel masking, sample skip, or custom implementations using the ADQ12 Development Kit.



Multi-record

Enables an exceptionally long pretrigger.

This mode is similar to triggered streaming. In addition, it allows for very long pretriggers; up to the entire record length. This allows for tracking and analyzing the cause of events. The parameters for multi-record data acquisition are found in **Table 9**. For pretrigger length below 16 kiSamples, us the Triggered streaming parameters. For pretrigger length above 16kiSamples use the multi-record parameters.

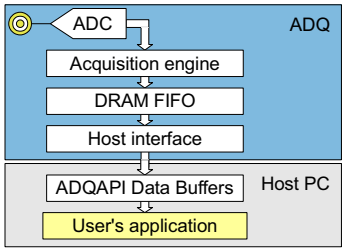


Data FIFO

Guarantees reliable data transfer.

The digitizer has 2 GBytes on-board DRAM, organized as a large FIFO. The FIFO guarantees stable operation over long time at high data rate. The FIFO also enable high trigger burst-rate.

13 Data Transfer

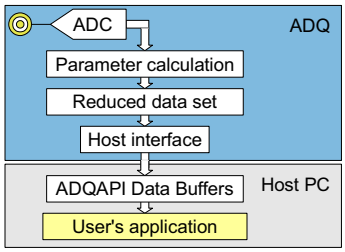


Data transfer with –FWDAQ

For maximum throughput to a powerful host PC.

The ADQ12DC hardware and software is designed for supporting high throughput to the host PC. The host PC interface is PCIe Generation2 x8 and supports up to 3.2 GBytes/s. The API supports efficient multi-threaded handling of data buffers (note that only one thread can communicate with the ADQ12DC hardware). There is example code for fast integration into the application.

All this enables efficient transfer to a powerful host PC where advanced application-specific computations are performed.



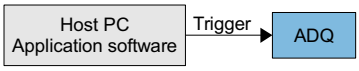
Real-time processing with –FWATD and –FWPD

Real-time processing for optimized data set.

The powerful real-time processing of the pulse detection firmware –FWPD and the averaging firmware –FWATD calculate descriptive parameters from the raw data stream. By transferring only these parameters and not all raw data, the amount of data is greatly reduced. The concept of calculating key parameters in the FPGA of the ADQ12DC is extended further by the open FPGA concept; ADQ12 Development Kit.

When the real-time processing is performed in the FPGA, the system can be designed around a compact host PC.

14 Trigger module



Software trigger

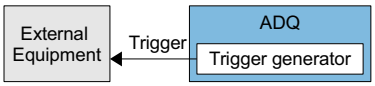
User-controlled triggering.

The software trigger is activated from the user's application software. It is used for building oscilloscope applications and for watchdog functions.

External trigger

Synchronizing the acquisition with external equipment.

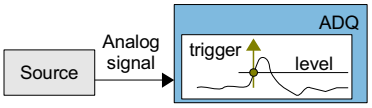
The external trigger is a signal from another unit that activates the acquisition. The external trigger is available on the front panel.



Internal trigger

Internally generated signal for triggering other devices.

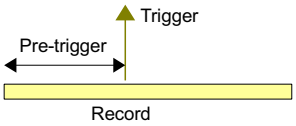
With the internal trigger, the ADQ12DC can be the timing master of a large system saving additional timing cards. The internal trigger generate a periodic trigger signal to other hardware units.



Level trigger

Data-driven triggering.

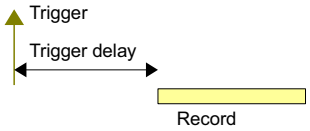
Activity on a data channel will trigger the acquisition. All channels are triggered simultaneously. More advanced level trigger functionality is included in the pulse detection firmware option –FWPD.



Pretrigger

Capturing data before the trigger event.

The pretrigger buffer allows for capturing data long before the trigger event occurred. This is useful for analyzing the cause of an event.

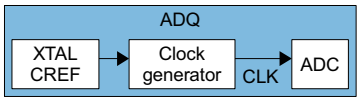


Trigger delay

Capturing data long after the trigger event occurred.

With this function the timespan for a measurement can be exceedingly large. By capturing only the event of interest, the amount of data is reduced.

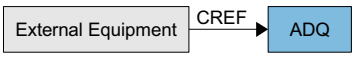
15 Clock module



Internal clock

High-precision clock for stand-alone operation.

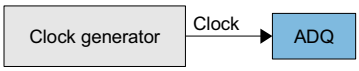
The internal clock is based on an internal high-precision reference source. The internal clock enables stand-alone operation.



External clock reference

Synchronize the acquisition to external equipment.

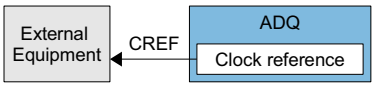
The digitizer can be synchronized with an experiment using the external clock reference. The internal clock generator gets its reference from an external source. There is a connector for this on the front panel.



External clock

Synchronize the acquisition to external equipment.

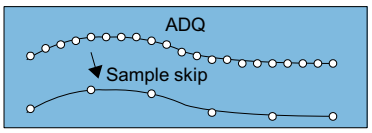
If an external clock is available, the ADQ12DC can be clocked directly by that source.



Clock reference output

Synchronize the acquisition to external equipment.

The digitizer can also be synchronized to external equipment using the clock reference output. ADQ12DC then acts as clock reference source for the entire system. The clock reference output can e.g. clock another ADQ12DC. This function together with the trigger generator can replace external timing cards.



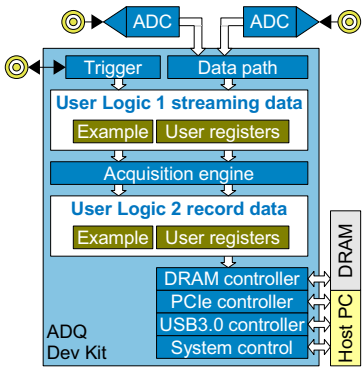
Sample skip[1]

Adapt the sample rate to the situation and minimize the amount of data.

The sample skip function can adapt the sample rate to the current situation and thus reduce the amount of data.The ADQ12DC can thereby easily adapt to changing conditions.

1. Sample skip can neither be combined with level trigger nor with firmware option –FWPD.

16 Feature enhancement options

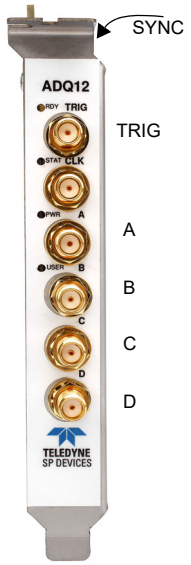


Real-time custom signal processing firmware through the ADQ12 Development Kit

The ADQ12DC is equipped with an powerful Xilinx Kintex 7 K325T FPGA which is partly available for customized real-time applications. SP Devices' ADQ12 Development Kit is an optional FPGA design project that enables custom real-time signal processing. More details about this product can be found in the datasheet for the ADQ12 Development Kit.

There are ADQ12 Development Kits available for the firmware options –FWDAQ and –FWPD. Note that the ADQ12 Development Kit is individual for each firmware option and purchased separately.

TRIG and SYNC can be used as GPIO



ADQ12DC–4C–SSPCIe

GPIO for connecting to external equipment

The General Purpose Digital Input Output (GPIO) is intended for communication with external equipment. It is accessed from the software through register read and write commands. Thereby, it can be used for creating a link between the external equipment and the user's software application.

Real-time interaction with the data flow is also possible through the ADQ12 Development Kit. Here, the GPIO signals are available in the User Logic area and can be used for interacting with the data in real-time.

The standard version of ADQ12DC has GPIO as a software selectable function on the TRIG and SYNC connectors.

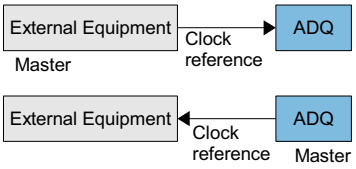
17 Data interface options

ADQ12DC–4C–SSPCIE

Systems integration with PCIe (–SSPCIE)

The PCIe form factor is for integration into the host PC. The board is available as single-slot (–SSPCIE) to save space in the PC cabinets.

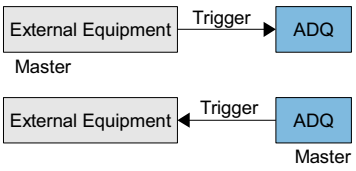
18 Synchronization support[1]



Clock reference input and output

Sharing clock reference guarantees a common timebase.

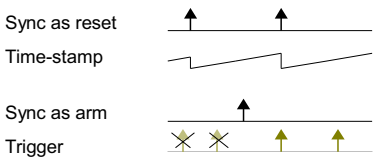
When outputting the internal clock reference, the ADQ12DC can act as a master. Alternatively, when the external equipment supplies the clock reference, the clock reference input can be used to achieve a common timebase.



Trigger input and output

The trigger starts the operation simultaneously.

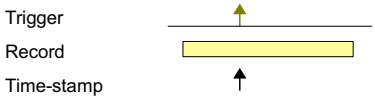
The trigger marks the start of an operation. The ADQ12DC can act as a master and generate a trigger to start external equipment. It can also take a trigger as input to start the acquisition.



Synchronization input and output

Extra trigger to mark beginning of a sequence.

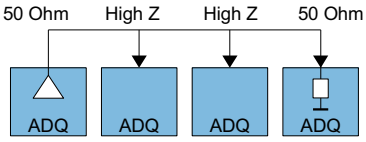
The sync pin is used for resetting the timestamp to mark the beginning of a sequence. The sync can also be used for broadcasting an arm command to several ADQ12DC units.



Timestamp

A real-time value for each trigger.

The timestamp is a real-time value for each trigger event. It can be used for comparing timing between events on the same board or from multiple boards.



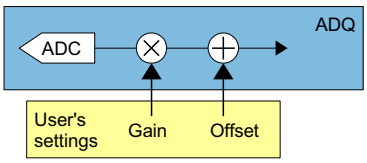
Bussed connection

Save cabling by bussed connections.

The sync, trig and clock reference can be set in high impedance mode to enable bussed connections. Note that the cable length has to be minimized to handle reflections.

1. See application note 15-1583 for more details.

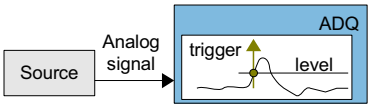
19 Built-in signal processing



Gain and offset calibration

Digital signal tuning in the FPGA.

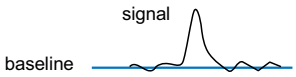
The gain and offset calibration can be used for optimizing the signal properties gain and offset in the FPGA to off-load the host computer. Note that this is a possibility to perform customized calibration performed by the user in order to optimize a certain system. Independently of this, the ADQ12DC is factory calibrated.



Level trigger

Data-driven acquisition.

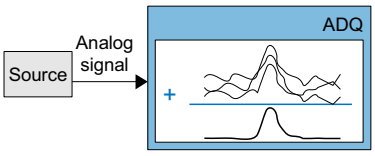
The standard firmware –FWDAQ contains a level trigger for data driven triggering and acquisition. For applications requiring advanced pulse detection and data analysis, the firmware option –FWPD is recommended.



Digital baseline stabilizer (DBS)

Enabling accurate pulse detection.

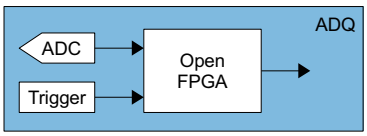
Teledyne SP Devices' proprietary technology for digital baseline stabilization, DBS, tracks baseline variations to suppress, for example, temperature drift in the detector of power supply fluctuations. The precision is as high as 22 bits, which efficiently suppresses e.g. pattern noise in time-interleaved solutions. DBS is available in firmware options –FWDAQ, –FWPD, and –FWATD.



Waveform averaging

Data reduction in scheduled repeated measurements.

The firmware option –FWATD offers averaging of waveforms for repeated measurements.



Custom real-time processing

Efficient algorithm implementation and short time-to-market.

The ADQ12 Development Kit opens the FPGA for custom implementation of real-time algorithms. Use Teledyne SP Devices' Design Service[1] for short time-to-market.

1. Contact an SP Devices' sales representative for more information.

20 Appendix

20.1 Cable attachment

All cables have a lock function so that no cable should fall out unintentionally.

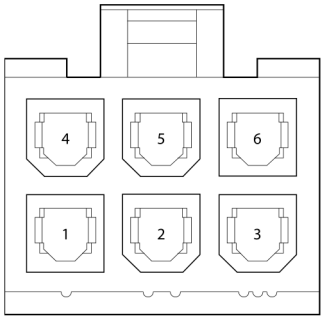
FUNCTION	CONNECTOR	LOCK FUNCTION
Analog	SMA	Screw
Trigger	SMA	Screw
Clock ref	SMA	Screw
Sync IN	MCX	Snap-lock placed inside PC chassis
Sync OUT	MCX	Snap-lock placed inside PC chassis
Power	PCIe Aux	Snap-lock
Data / control	Backplane	Screw to attach the board in chassis

20.2 LED definitions

NAME	COLOR	FUNCTION	STATE
PWR	Green	Power on	On: Power on and FPGA is operating
RDY	Yellow	Waiting for trigger	Set up to accept trigger and waiting for the trigger
STAT	Red	Overheat	Flashing means overheating or fan fault.
USER	Blue	Custom	On during initialization of the board. Available for custom implementation in ADQ12 Development Kit

20.3 Host interface –SSPCIE

The ADQ12DC–SSPCIE is powered from the power supply of the PC via a PCI Express 6-pin (2x3) auxiliary power supply connector, **Figure 8**. The connection in the cable should be as in **Figure 7**. It is important that the axillary power supply is turned on immediately when the PC start. Otherwise, the digitizer will not be recognized on the PCI Express bus.



(a) Cable connection

Pin	Signal
1	+12 V
2	+12 V
3	+12 V
4	Ground
5	Sense
6	Ground

(b) Pin-out table

Figure 7: Power supply of –SSPCIE

Figure 8: Installation in a PC cabinet. Note the power cable and the SYNC in and out connectors. The USB connector is for firmware upgrade.

Ordering information

ORDERING INFORMATION	
ADQ12DC DC-coupled	ADQ12DC
AVAILABLE OPTIONS	
Host PC interface	–SSPCIE
Analog front-end options	–2C, –4C
Firmware options	–FWDAQ, –FWATD, –FWPD
RELATED PRODUCTS	
ADQ12 Development Kit for –FWDAQ	ADQ12 Development Kit –FWDAQ
ADQ12 Development Kit for –FWPD	ADQ12 Development Kit –FWPD

References

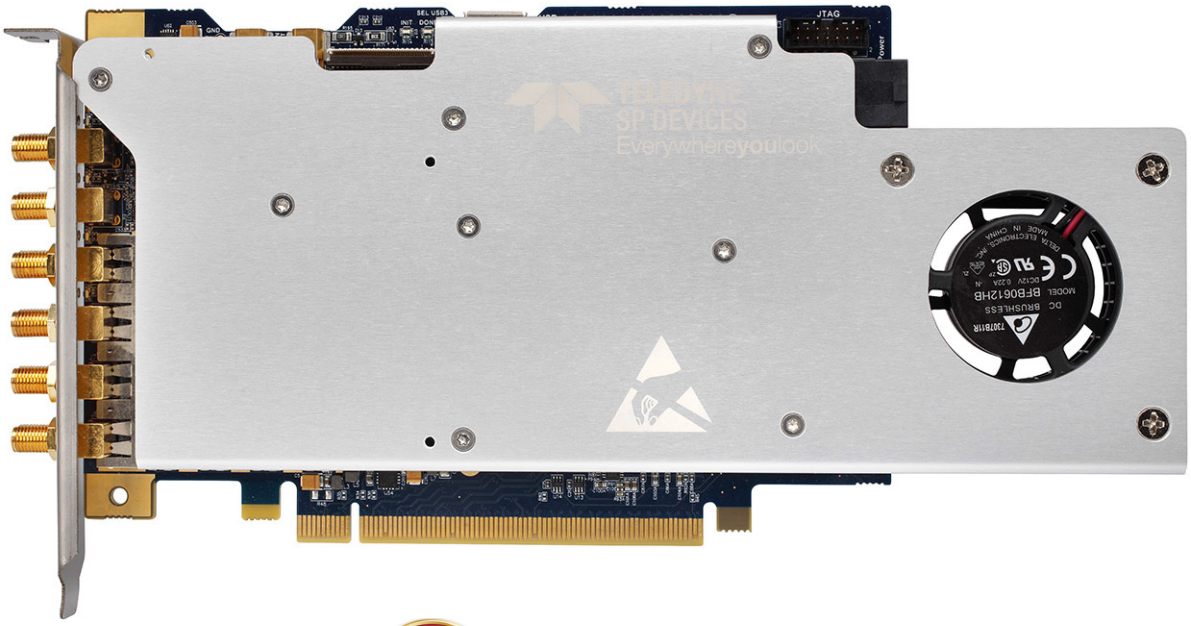
18-2199 ADQ12DC manual

14-1397 ADQ14-FWATD datasheet

15-1455 ADQ14-FWPD datasheet

14-1351 ADQAPI reference guide

15-1583 ADQ14 Synchronizing Several Units



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