ADQ35 Datasheet

The ADQ35 is a high-end 12-bit dual-channel data acquisition board optimized for use in high-throughput scientific applications. The ADQ35 features:

- **One analog channel at 10 GSPS**
- **Two analog channels at 5 GSPS per channel**
- **Sampling rate option at 8 GSPS and 4 GSPS respectively**
- **12 bits resolution**
- **14 GByte/s sustained data transfer rate to GPU**
- **14 GByte/s sustained data transfer rate to CPU**
- **Two external triggers**
- **General Purpose Input/Output (GPIO)**
- **Open FPGA for real-time signal processing**
- **Firmware option for averaging of records**
- **Firmware option for pulse analysis**

1 ORDERING INFORMATION

ADQ35 is available with a set of options. Follow the procedure to configure the ADQ35. Start with the hardware configurations. These are factory installed and cannot be changed through software commands.

1. Select the DC-coupled analog front-end **-DC** (standard). For dual-gain **-PDRX** analog front-end, see 22-2919 ADQ35-PDRX datasheet[1].

Select the firmware options, see section 5 for details. The firmware FWDAQ is always included. Additional firmware options are distributed as files and can be loaded into the board at any time.

2. Data acquisition firmware **-FWDAQ** is always included
3. Select one or several optional firmware packages, **-FWATD**, **-FWPD**.
4. Select to activate channel combination option for dual-gain pulse detection, **-LICPDRX**[2].
5. Select accessories, open FPGA development kit **DEVDAQ**, **-DEVPD**[3].
6. Select extended warranty **-W5Y**.

The open FPGA is accessed through the design project for each firmware. For **-FWDAQ**, the development kit is **DEVDAQ**. The FPGA bit files built from the design project using **DEVDAQ** can be used on any ADQ35 with a valid **FWDAQ** license (included on all units).

For **-FWPD**, the development kit is **DEVPD**. The FPGA bit files built from the design project using **DEVPD** can be used on any ADQ35 with a valid **FWPD** license.

The **DEVDAQ** and **DEVPD** are one-time purchases.

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[1] Contact Teledyne SP Devices for information about availability.

[2] See 22-2797 ADQ35-PDRX datasheet for more information about dual-gain channel combination. The ADQ35 can be used with external dual-gain amplifier and channel combination in firmware. The option LICPDRX activates the channel combination for external dual-gain amplifier.

[3] DEVPD is available in 2024. Contact Teledyne SP Devices for more information.

2 ADQ35 INTRODUCTION

2.1 Features

- One and two analog input channels
- 10 or 8 GSPS sampling rates in single channel mode
- 5 or 4 GSPS sampling rate per channel in dual channel mode
- 12 bits resolution
- DC-coupled with 2.5 GHz bandwidth
- Programmable DC-offset
- Internal and external clock reference
- Clock reference output
- Internal and external triggers
- 8 Gbyte data memory
- 14 GByte/s sustained data streaming to CPU and GPU
- Data format 16-bit MSB aligned or rounded to 8-bit
- Data interface PCIe Gen3 x16
- Averaging firmware FWATD
- Pulse analysis firmware FWPD

2.2 Applications

- Swept-source optical coherence tomography (SS-OCT)
- Time-of-flight mass spectrometry
- Distributed optical fiber sensing
- LIDAR
- Scientific instruments
- Scanning acoustic microscopy

2.3 Advantages

- A space-saving, single-slot, high-performance digitizer supporting up to 55°C ambient for demanding industrial applications
- Real-time processing and high data throughput
- Teledyne SP Devices' design services are available for fast integration to reduce time-to-market

2.4 System design optimization; open FPGA and streaming to CPU and GPU

High-performance data acquisition systems require high speed real-time analysis. ADQ35 offers a variety of options for efficient system design:

Streaming to GPU
ADQ35 supports up to 14 GByte/s peer-to-peer streaming and streaming via pinned buffer to GPU. A GPU offers a powerful platform for implementing application-specific signal processing algorithms.

Streaming to CPU
ADQ35 supports up to 14 GByte/s to host computer. Implementing the application-specific algorithms in the CPU results in an efficient system.

Open FPGA for real-time processing
ADQ35 offers an open FPGA for implementation of the application-specific computations in the FPGA. This gives the most compact system design. Firmware development kit is ordered separately.

Pulse data recording
The hardware option ADQ35-PDRX offers a built-in dual-gain amplifier for pulse data capture with extended dynamic range. See datasheet 22-2919 for more details on the option ADQ35-PDRX.

3 TECHNICAL DATA

Technical parameters are valid for ADQ35 operating with firmware FWDAQ. All parameters are typical unless otherwise noted.

Table 1 Analog input (front panel A and B)

Parameter	Condition	Min	Typical	Max	Unit
Basic parameters					
Bandwidth -3dB			2.5		GHz
Input range			0.5		Vpp
Input impedance			50		Ω
Coupling			DC		
Connector type			SMA		
Programmable DC-offset					
DC-offset range		-0.25		+0.25	V
Dynamic performance 2 channels mode at 5 GSPS					
Cross talk	< 2.5 GHz		-63		dBc
Noise power density	0 to 2.5 GHz		-147		dBFS/√Hz
SNR	260 MHz, -1dBFS		52		dBc
SFDR	260 MHz, -1dBFS		63		dBc
ENOB relative full scale	10 MHz, -1dBFS		8.4		bits
ENOB relative full scale	260 MHz, -1dBFS		8.4		bits
ENOB relative full scale	810 MHz, -1dBFS		8.4		bits
ENOB relative full scale	1625MHz,-1dBFS		8.3		bits
Dynamic performance, 2 channels mode at 5 GSPS, FIR filter bandwidth 1.25 GHz[4]					
ENOB relative full scale	810 MHz, -1dBFS	bits	8.8		bits
Dynamic performance, 1 channel mode at 10 GSPS, connector A[5]					
Noise power density	0 to 5 GHz		-150		dBFS/√Hz
SNR	260 MHz, -1dBFS		51		dBc
SFDR	260 MHz, -1dBFS		61		dBc
ENOB relative full scale	10 MHz, -1dBFS		8.4		bits
ENOB relative full scale	260 MHz, -1dBFS		8.3		bits
ENOB relative full scale	810MHz,-1dBFS		8.3		bits
ENOB relative full scale	1625MHz,-1dBFS		8.2		bits
Dynamic performance, 1 channel mode at 10 GSPS, FIR filter bandwidth 2.5 GHz, connector A[5]					
ENOB relative full scale	260 MHz, -1dBFS		8.7		bits
ENOB relative full scale	810 MHz, -1dBFS		8.7		bits

[4] Built-in user-programmable digital FIR filter; symmetrical, 17 taps. Filter coefficients used for this test are [57, 92, –279, 21, 704, –720, –1163, 4127, 10784] / 2^{14}.

[5] Performance parameters are valid for 1 channel mode using input A. It is possible to use channel B as input but there are no parameters available for 1 channel mode using input connector B.

Table 2 Clock generator and front panel CLK connector

Parameter	Condition	Min	Typical	Max	Unit
Internal clock reference					
Frequency			10		MHz
Accuracy			±3 ±1/year		ppm
Internal sampling clock generator [6] [7]					
Frequency range 1	2 channels	4990	5000	5010	MHz
Frequency range 2	2 channels	3990	4000	4010	MHz
Frequency range 3	2 channels	2990	3000	2010	MHz
Frequency range 1	1 channel	9980	10000	10020	MHz
Frequency range 2	1 channel	7980	8000	8020	MHz
Frequency range 3	1 channel	6980	6000	6020	MHz
External clock reference input (from front panel CLK connector)[8]					
Frequency		1	10	500	MHz
Frequency [9]	Jitter cleaner enabled	10 -50 ppm	10	500 +50 ppm	MHz
Frequency	Delay line used		10	100	MHz
Delay line tuning range			500		ps
Signal level		0.5		3.3	Vpp
Input impedance	AC		50		Ω
Input impedance	DC		10k		Ω
Input impedance (high) [10]	AC		200		Ω
Clock reference output (on front panel CLK connector)[11]					
Frequency			10		MHz
Signal level	Into 50-Ω load		1.2		Vpp
Output impedance	AC		50		Ω
Output impedance	DC		10k		Ω
Physical connector label CLK					
Connector type		SMA			

[6] The internal clock generator can generate frequencies in 3 different ranges.
[7] The software setting is limited to the typical value. The tolerance min-max is the limits with external clock reference that deviate from its nominal value.
[8] Using a clock reference from an external source to synchronize the ADQ35 to the external source.
[9] The jitter cleaner requires the reference frequency to be a multiple of 10 MHz within ± 10ppm.
[10] Software-selectable high-impedance mode.
[11] The internal clock reference of the ADQ35 is made available to synchronize external equipment.

Table 3 Front panel TRIG connector

Parameter	Condition	Min	Typical	Max	Unit
Connector type		SMA			
Used as input (trigger or general-purpose input, GPI)					
Impedance	DC		50		Ω
Impedance (high) [12]	DC		500		Ω
Signal level	50-Ω mode	-0.5		3.3	V
Adjustable threshold	50-Ω mode	0		2.8	V
Signal level	High impedance	-0.5		5.5	V
Adjustable threshold	High impedance	0		2.3	V
Pulse repetition frequency	As trigger			10	MHz
Time resolution [13]	As trigger		50		ps
Update rate [13]	As GPI			156.25	MHz
Used as output (trigger or general-purpose output, GPO)					
Impedance	DC		50		Ω
Output level high VOH	Into 50-Ω load	1.8			V
Output level low VOL	Into 50-Ω load			0.1	V
Pulse repetition frequency				156.25	MHz

Table 4 Front panel SYNC connector (may be used as a trigger source with larger timing grid)

Parameter	Condition	Min	Typical	Max	Unit
Connector type			SMA		
Used as input (trigger or general-purpose input, GPI)					
Impedance	DC		50		Ω
Impedance (high) [12]	DC		500		Ω
Signal range	50-Ω mode	-0.5		3.3	V
Adjustable threshold	50-Ω mode	0		2.8	V
Signal level	High impedance	-0.5		5.5	V
Adjustable threshold	High impedance	0		2.3	V
Pulse repetition frequency	As trigger			10	MHz
Time resolution [13]	As trigger		3.2		ns
Update rate [13]	As GPI			156.25	MHz
Used as output (trigger or general-purpose output, GPO)					
Impedance	DC		50		Ω
Output level high VOH	Into 50-Ω load	1.8			V
Output level low VOL	Into 50-Ω load			0.1	V
Pulse repetition frequency				156.25	MHz

[12] Software-selectable high-impedance mode.

[13] Timing properties are valid for 5 GSPS in 2 channel mode and 10 GSPS in 1 channel mode. Timing properties scale linearly with sampling frequency.

Table 5 Front panel GPIO connector (general purpose input/output)

Parameter	Condition	Min	Typical	Max	Unit
Connector type			SMA		
Used as input					
Impedance			50		Ω
Impedance (high) [12]			10		kΩ
Input level high VIH		2			V
Input level low VIL				0.8	V
Update rate [13]				156.25	MHz
Used as output					
Output Impedance			50		Ω
Output level high VOH	Into 50-Ω load	1.5			V
Output level high VOH	No load	3.2			V
Output level low VOL	Into 50-Ω load			0.1	V
Output level low VOL	No load			0.1	V
Update rate [13]				156.25	MHz

Table 6 Environmental and mechanical parameters

Parameter	Condition	Min	Typical	Max	Unit
Power and temperature					
Power consumption [14]	FWDAQ		48		W
Power supply		10.8	12	13.2	V
Operating temperature	FWDAQ[15]	0		55	°C
Operating temperature	FW options[16]	0		45	°C
Size					
Width 1 slot			18.42		mm
Length			269.55		mm
Height			111.15		mm
Weight			600		g
Compliances					
RoHS3		Yes			
CE		Yes			
FCC	Exclusion according to CFR 47, part 15, paragraph 15.103(c).				

[14] Power consumption depends on firmware option and use case. Power consumption is measured during acquisition and streaming of data at 14 Gbyte/s to PC.

[15] Operating the ADQ35 with FWDAQ and streaming data up to 14 Gbyte/s.

[16] Using firmware options from Teledyne SP Devices. Custom firmware designs may result in higher power consumption and thereby lower temperature range.

Table 7 Custom GPIO expansion. See section 10.

Parameter	Value
Connector type	40-pin FFC/FPC connector, pitch 0.5 mm
Number of differential IO signals LVDS	8
Number of single-ended IO signals 3.3V	5

Table 8 Data acquisition

Parameter	Condition	Min	Typical	Max	Unit
Rearm time[17]				20	ns
Acquisition memory (Data FIFO)	Shared by all channels		8		Gbyte
Record length	2-channel mode in steps of 1	2		2^{32}-1	samples
	1-channel mode in steps of 1	2		2^{32}-1	samples
Pre-trigger[18]	2-channel mode in steps of 16	0		16 336	samples
	1-channel mode in steps of 32	0		16 228	samples
Trigger delay[19]	2-channel mode in steps of 16	0		2^{36}-16	samples
	1-channel mode in steps of 32	0		2^{37}-32	samples

Table 9 Data transfer[20]

Parameter	Value	Unit
Supported versions of data transfer standard PCIe	Gen1 / Gen2 / Gen3	
Supported number of lanes[21] [22]	1 / 4 / 8 / 16	
Data rate to CPU sustained	14	GByte/s
Data rate to GPU sustained	14	GByte/s
Data rate peer-to-peer to GPU sustained	14	GByte/s
Data format[23]	32 / 16 / 8	bits

[17] Minimum time from the last sample of a record to the next trigger.
[18] Pre-trigger is set by assigning the parameter “horizontal offset” a negative value
[19] Trigger delay is set by assigning the parameter “horizontal offset” a positive value
[20] This is the data rate that the ADQ35 supports. Other parts of the system may limit the performance.
[21] The ADQ35 must be installed in a 16 lanes slot or a slot with a connector with an open end. If a shorter connector is used, the number of lanes and the maximum data rate is limited.
[22] PCIe bifurcation is required for 16 lanes
[23] Default 16 bits MSB-aligned.

Table 10 Software support

Parameter	Value
Operating system[24]	Windows / Linux
GUI	Digitizer Studio
Example code	C, Python
API	C / C++
High-level API	LabVIEW / MATLAB / C#

4 FEATURES FOR DATA FLOW CONTROL, SYNCHRONIZATION AND PROCESSING

The ADQ35 features an advanced machine for flow control, synchronization, and signal processing. The block diagrams are shown in Figure 1 and Figure 2. The features are described in the following tables.

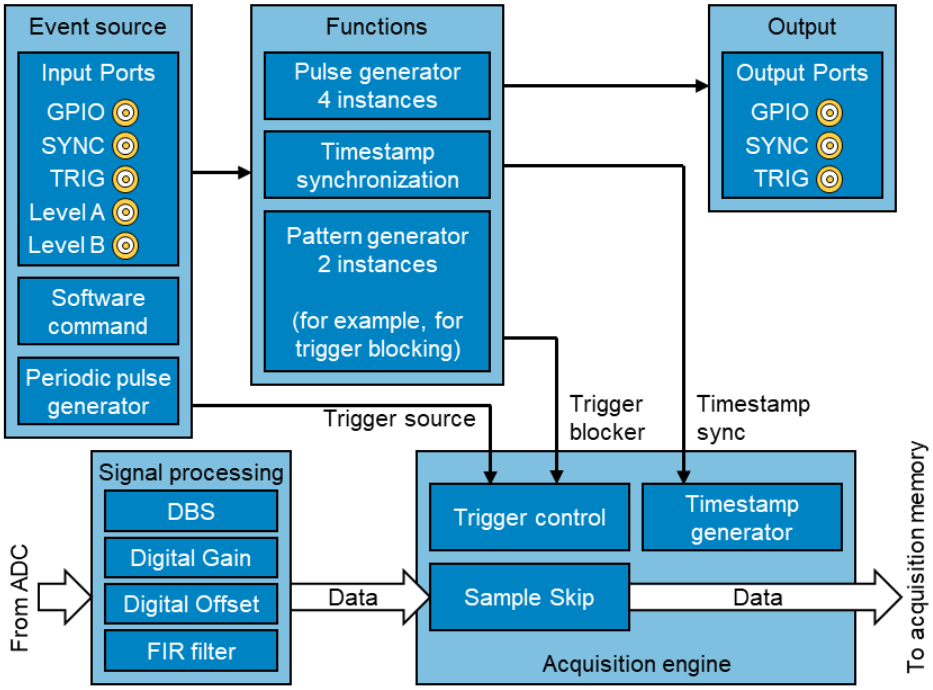

Figure 1 Flow control and synchronization block diagram.

Table 11 Digital signal processing blocks

Object type	Available selections
Digital Signal Processing Included signal processing in the data path for enhanced signal quality.	Digital Baseline Stabilizer (DBS) Digital gain Digital offset Digital FIR filter

[24] See 15-1494 Operating system support for a detailed listing of supported distributions.

Table 12 Flow control blocks

Object type	Available selections
Input ports Electrical connections to the ADQ35 for real-time operation (excluding the PCIe data interface) Used as event source.	Front panel TRIG Front panel SYNC Front panel GPIO Front panel CLK (clock reference or clock input only) Analog channel A Analog channel B
Event sources Signals for real-time control of activities in the firmware of ADQ35.	Software command External TRIG External SYNC External GPIO Internal periodic event generator Level analog channel A Level analog channel B
Functions Included operations for real-time control of activities in the firmware of ADQ35.	Pattern generator for timestamp synchronization Pattern generator general purpose, 2 instances Pulse generator, 4 instances
Output ports Electrical connections to the ADQ35 for real-time operation (excluding the PCIe data interface).	Front panel TRIG Front panel SYNC Front panel GPIO Front panel CLK (clock reference output only)

Table 13 Firmware functions for flow control

Function	Modes/selections	Event sources as stimuli
Pattern generator for timestamp synchronization Control the time of the ADQ35.		Software command External TRIG External SYNC Internal periodic event generator
Pulse generator Control output pulse shapes. Three instances.	Rising edge Falling edge Pulse length Polarity	Software command External TRIG External SYNC Internal periodic event generator
Pattern generator general purpose For example, used for trigger blocking.	Once Window Gate Trigger counter	Software command External TRIG External SYNC Internal periodic event generator

Table 14 Firmware functions for acquisition

Function	Modes	Event Sources as stimuli / control
Trigger Initiate the acquisition of a data record.		Software command External TRIG External SYNC Internal periodic event generator Level analog channel A Level analog channel B
Data acquisition modes Configurations for sending digital data to the host PC.	Fixed record length Dynamic record length (zero suppression)	Selected **Trigger** for initiating data acquisition
Data transfer modes Transport to CPU / GPU	Streaming with header Streaming without header	User set-up

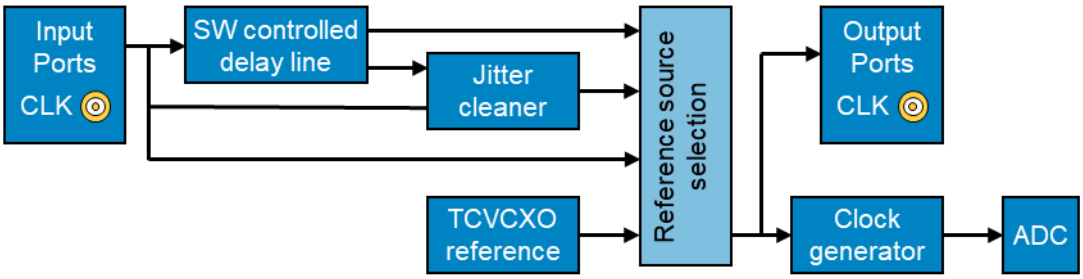

Figure 2 Clock generation block diagram.

Table 15 Clock generation

Function	Modes
Clock reference source Phase and frequency reference for the clock system.	Internal TCVCXO External External with jitter cleaner and/or delay line
Sampling clock sources Actual clock for taking the samples of the analog data.	Internal clock generator
Clock output	Selected clock reference source

5 FIRMWARE

5.1 FWDAQ

The FWDAQ is included with all digitizers. The firmware includes control of the hardware and recording of data.

The dual-gain channel combination included in FWDAQ requires a separate license for ADQ35.

5.2 FWATD

The FWATD is optional. It includes thresholding for noise suppression and accumulations of waveforms. See datasheet 22-2912 for more details.

The dual-gain channel combination included in FWATD requires a separate license for ADQ35.

5.3 FWPD

The FWPD is optional. It includes detection and analysis of pulses. See datasheet 23-3028 for more details.

The dual-gain channel combination is included in FWPD requires a separate license for ADQ35.

5.4 Managing firmware

The digitizer supports multiple firmware images. Note the following about managing firmware images:

- The non-volatile memory on the digitizer can store up to four different firmware images (including the active firmware). Use the tool ADQAssist to change firmware and to upload new images to the digitizer.
- Each hardware can include a license for multiple firmware options. If all firmware images cannot be stored on the device, some may need be stored on the host computer for manual reprogramming via ADQAssist.
- The digitizer (and the enclosing host computer) must be power cycled for the firmware switch to be completed. This is required to let the PCIe bus enumerate with the new firmware.
- Some firmware features require a valid license key to activate. See the ordering information section for details about available firmware features.
- Switching mode between one channel at 10 GSPS and two channels at 5 GSPS requires switching the digitizer firmware image.

6 ABSLOUTE MAXIMUM RATINGS

Table 16 Absolute maximum ratings

Parameter	Condition	Min	Max	Unit
Power supply to GND		-0.4	14	V
Operating temperature[25]		0	55	°C
Storage temperature		-40	70	°C
Analog in to GND		-2.5	+2.5	V
TRIG to GND	50-Ω mode	-2	5	V
SYNC to GND	50-Ω mode	-2	5	V
TRIG to GND	500-Ω mode	-2	6	V
SYNC to GND	500-Ω mode	-2	6	V
CLK REF to GND AC amplitude			5	Vpp
CLK REF to GND DC-level		-5	5	V
GPIO to GND		-1.5	5	V
FFC / FPC differential signal to GND	Powered[26]	-0.5	2.3	V
	Not powered[26]	-0.5	0.5	V
FFC / FPC single-ended signal to GND [26]	Powered[26]	-0.3	3.8	V
	Not powered[26]	-0.3	0.5	V

Exposure to conditions exceeding these ratings may reduce lifetime or permanently damage the digitizer. The digitizer with PCIe format has a built-in fan to cool the device. The built-in temperature monitoring unit will protect the digitizer from overheating by temporarily shutting down parts of the device in an overheat situation.
The SMA connectors have an expected lifetime of 500 operations. For frequent connecting and disconnecting of cables, connector savers are recommended.

[25] The absolute maximum temperature is the range where it is allowed to start the board.
The ADQ35 has a built-in overheat protection to prevent damage from overheat. The ADQ35 may therefore shut down at lower temperature than the absolute maximum.
The overheat conditions is depending on the load of the FPGA. For Teledyne SP Devices provided firmware options, see recommended operating conditions in Table 6. For custom firmware the temperature range must be evaluated from case to case.

[26] The absolute maximum ratings depend on whether the ADQ35 is powered or not. It is recommended to use the respective power rail in the FFC connector to power or enable the external drivers to avoid driving overvoltage into an unpowered digitizer. Use the 1.8 V rail for the differential signals and 3.3 V for the single-ended signals.

7 TYPICAL PERFORMANCE

7.1 Frequency response

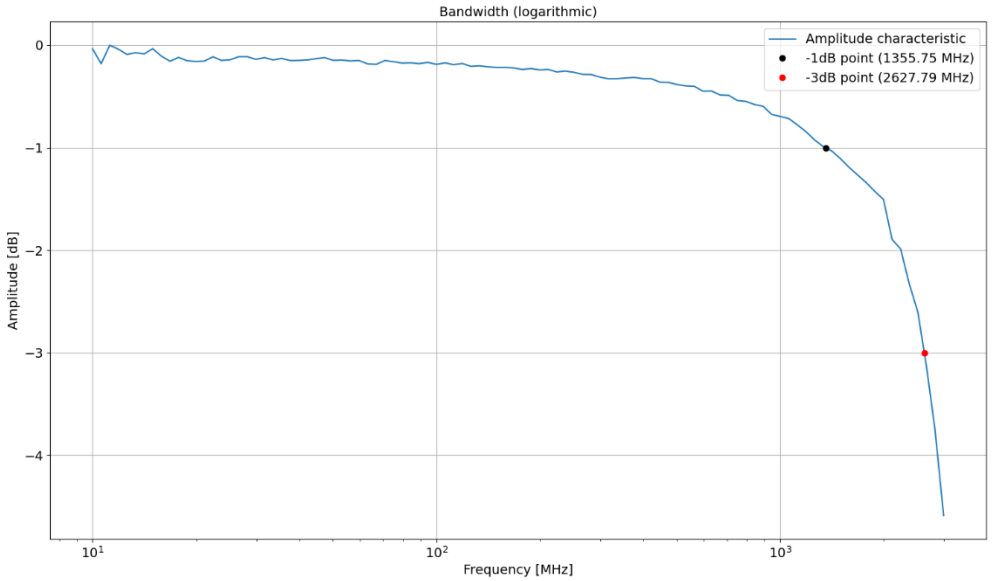

Figure 3 Frequency response, logarithmic frequency scale.

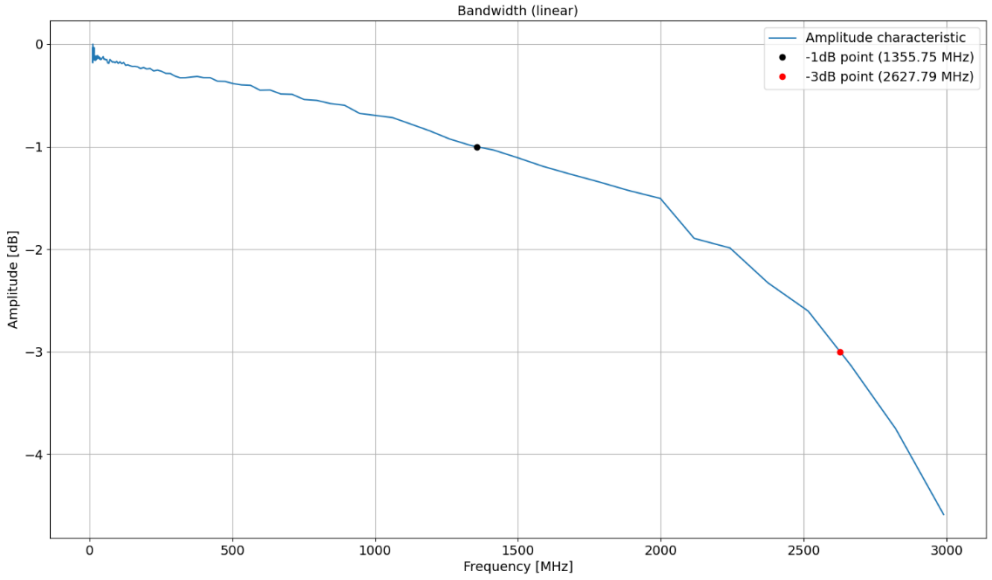

Figure 4 Frequency response, linear frequency scale.

7.2 FFT

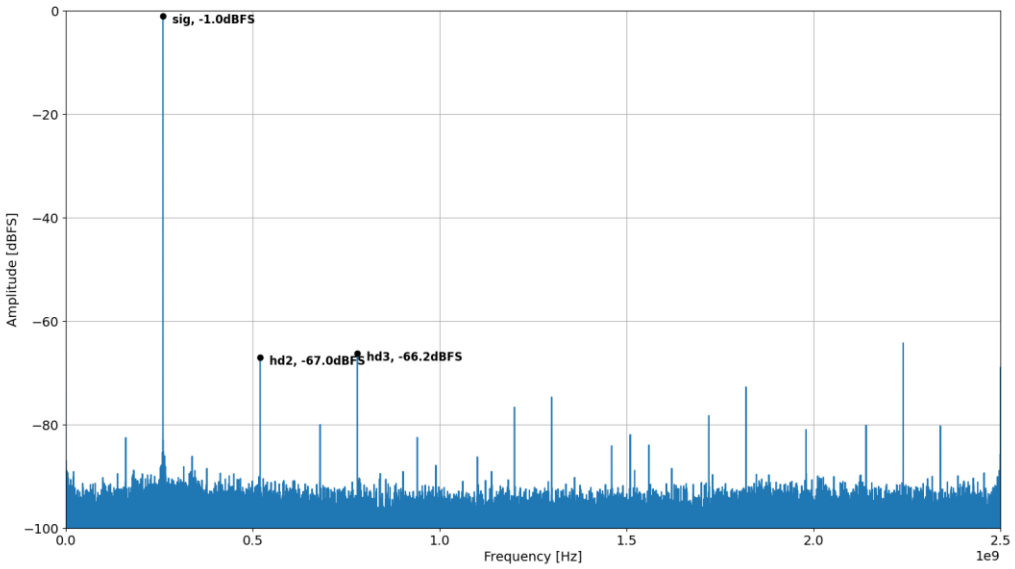

Figure 5 FFT typical performance 5 GSPS.

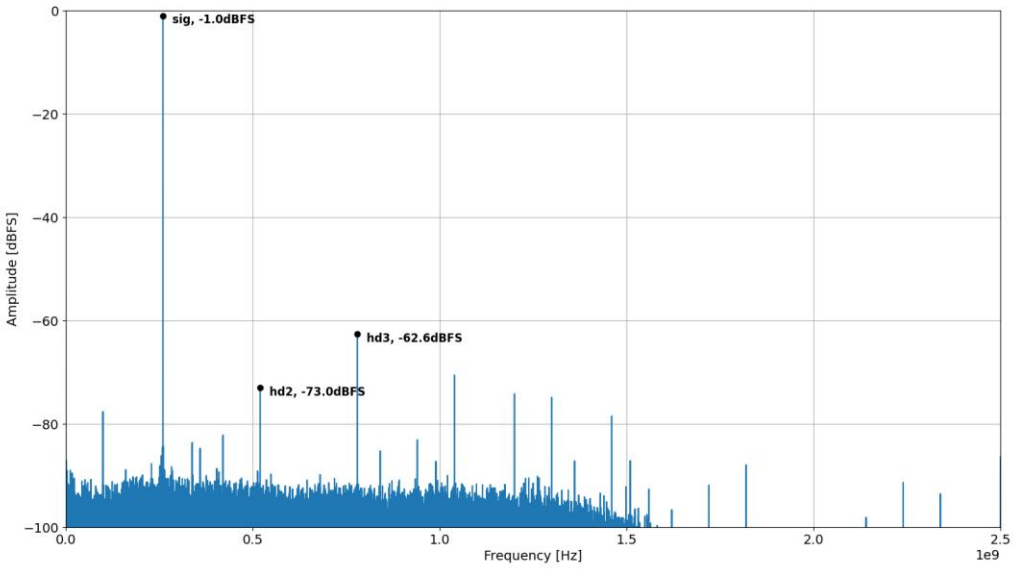

Figure 6 FFT typical performance 5 GSPS using FIR filter.

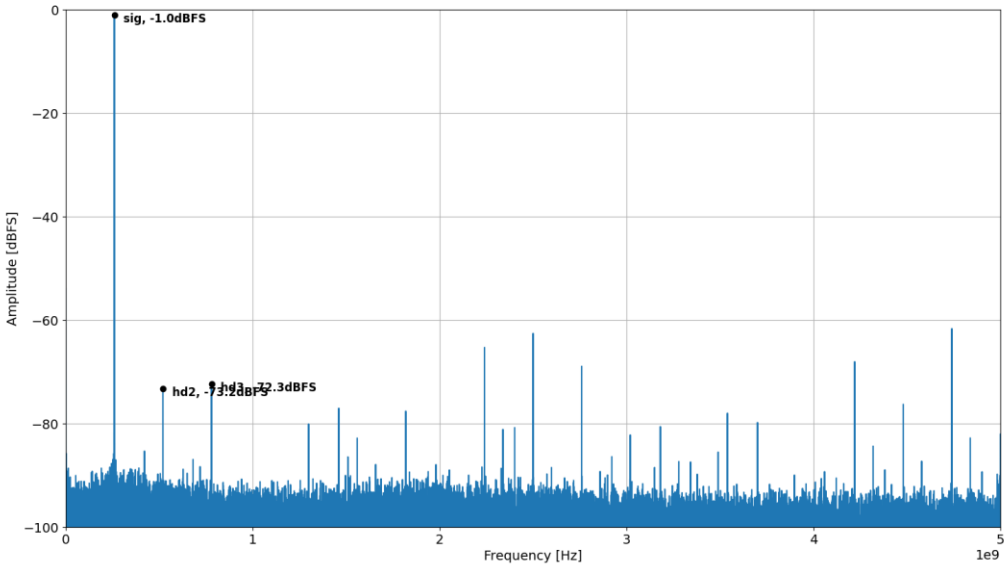

Figure 7 FFT typical performance at 10 GSPS.

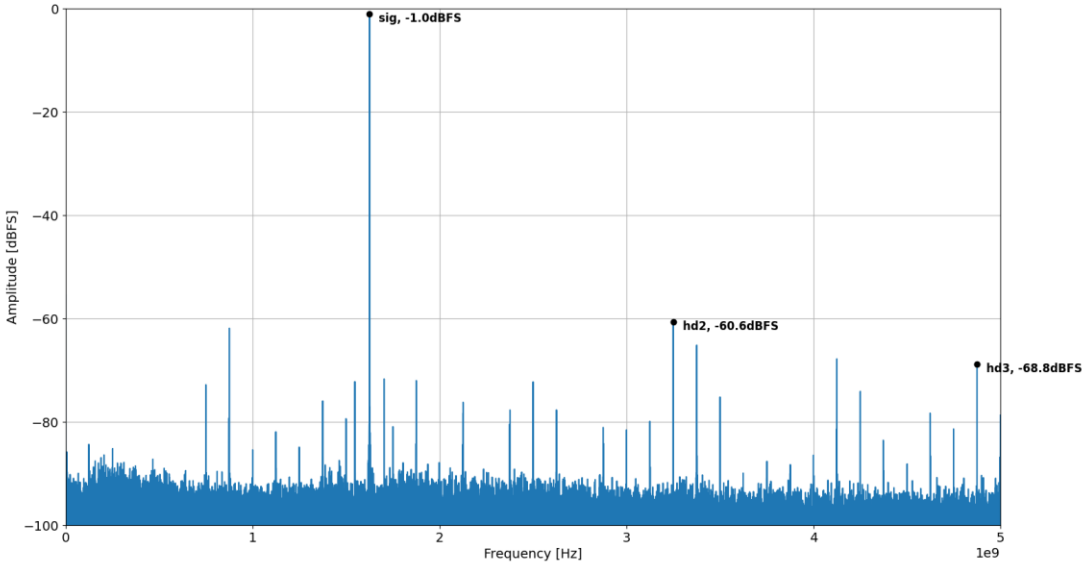

Figure 8 FFT typical performance 10 GSPS.

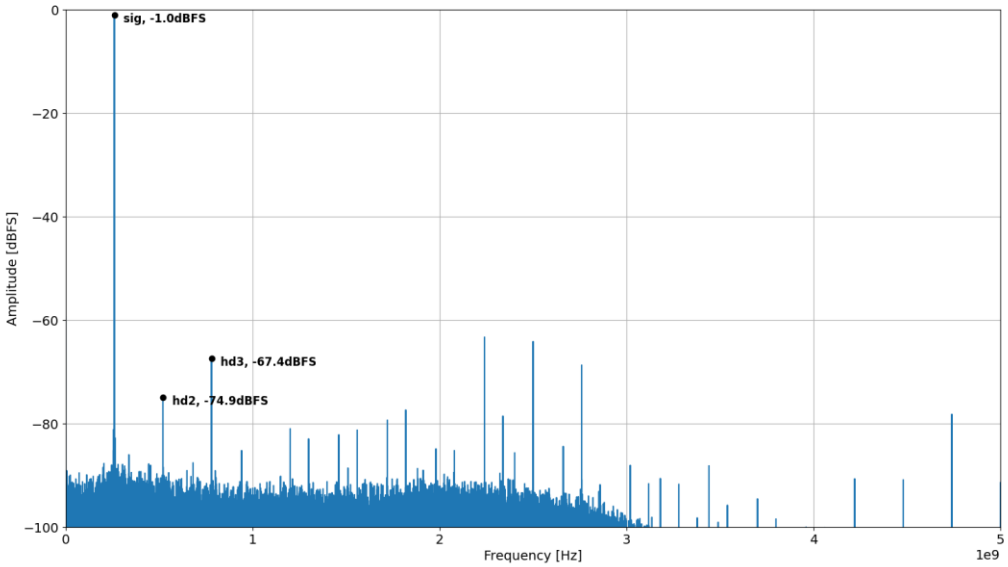

Figure 9 FFT typical performance 10 GSPS using FIR filter.

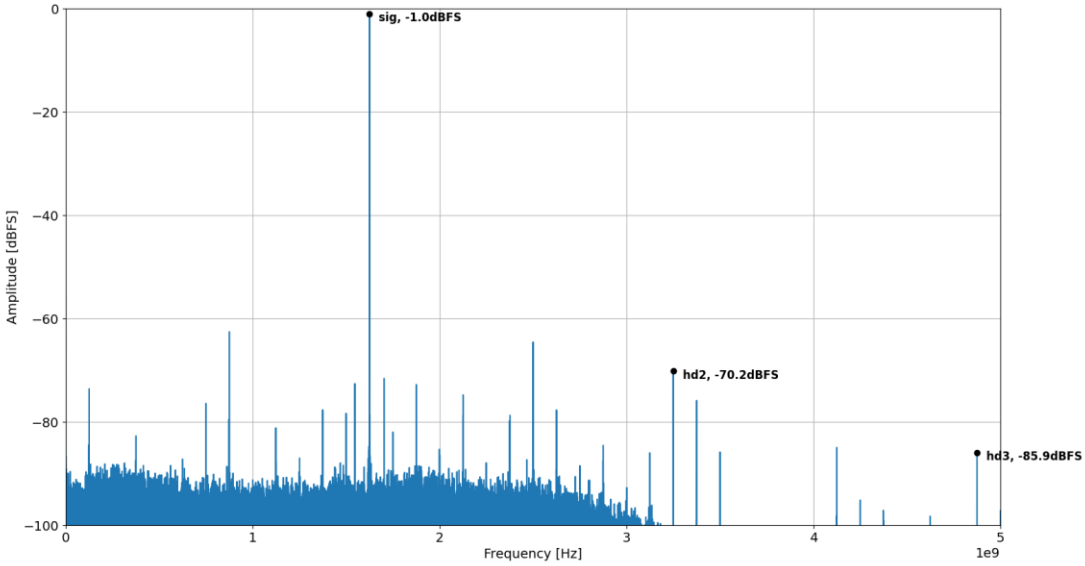

Figure 10 FFT typical performance 10 GSPS using FIR filter.

8 BLOCK DIAGRAM

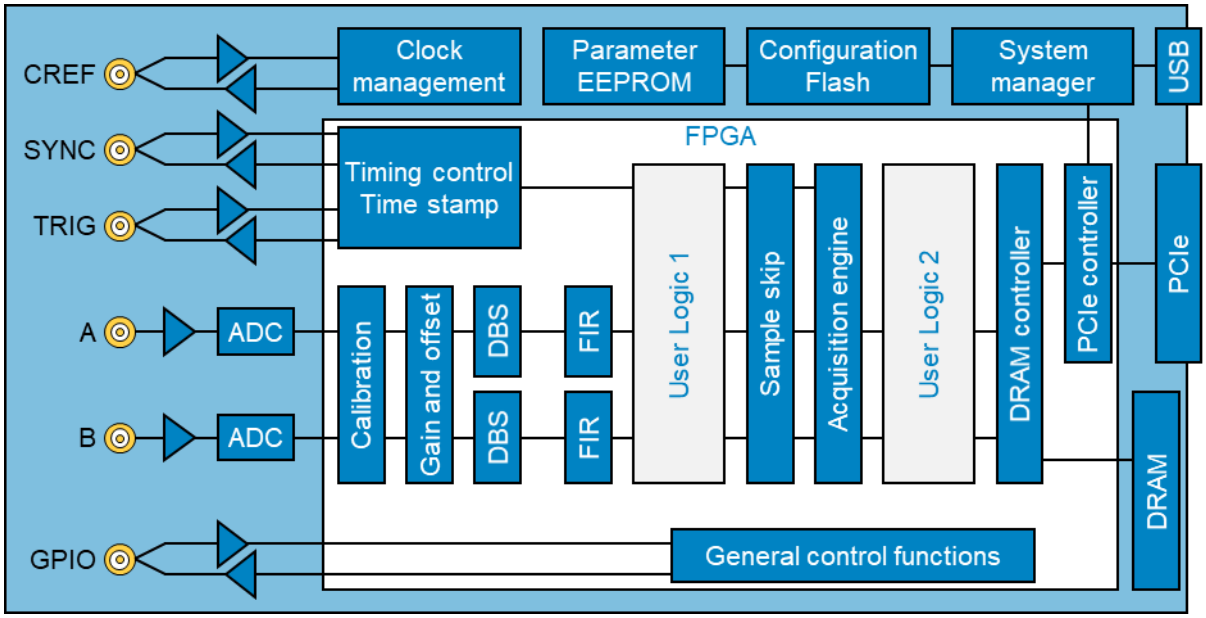

Figure 11 Block diagram.

Figure 11 shows a block diagram of ADQ35 in 2-channel mode. The blocks marked “User Logic” are open for custom real-signal processing thought the firmware development kit (purchased separately).

9 HOST PC INTERFACE PCIE

The ADQ35-PCIe is powered from the power supply of the PC via a PCI Express 8-pin (2x4) auxiliary power supply connector. The connection in the cable should be as in Figure 12. It is also possible to operate the board from a PCI Express 6-pin (2x3) auxiliary power supply connector. Consider the power ratings for the respective connectors from the PC manufacturer.

It is important that the auxiliary power supply is turned on immediately when the PC starts. Otherwise, the digitizer will not be recognized on the PCI Express bus.

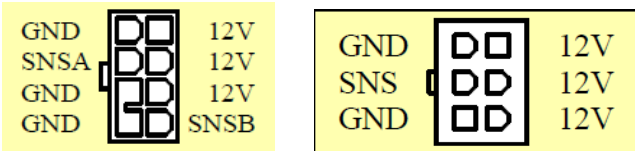

Figure 12 Power supply connection options. PCB connector.

10 GPIO EXPANSION

The FCP connector allows direct access to the FPGA for building custom expansion boards. The FCP connector requires custom firmware and is accessible through the FPGA development kit. The ADQ3 series user guide document number 21-2539 contains a description of connector.

Note that this connector is connected directly to the FPGA. Damage caused by custom hardware failure is not covered by warranty.

Contact Teledyne SP Devices' sales representative for more information.

11 MECHANICAL DRAWING

Figure 13 Photo of ADQ35.

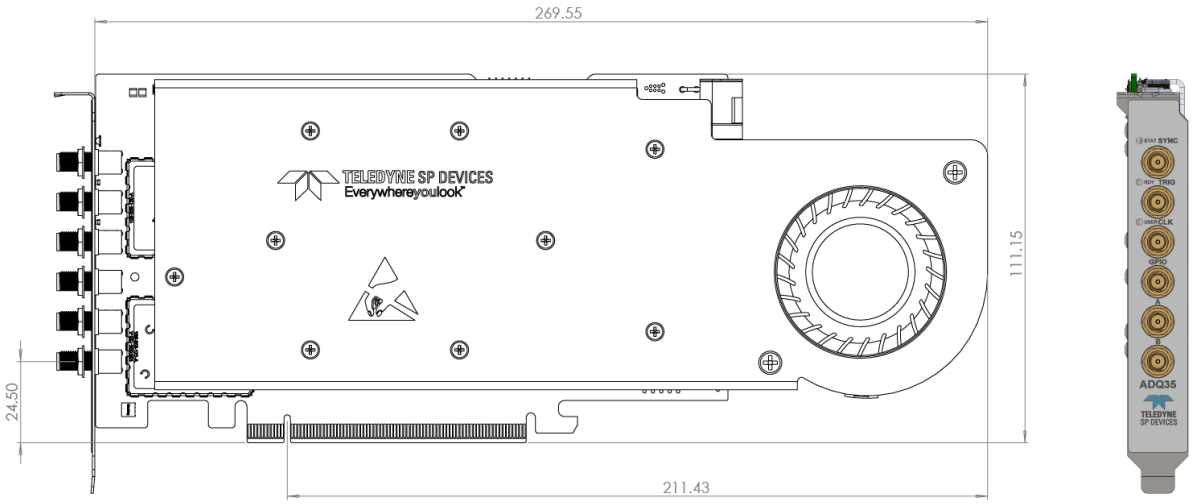

Figure 14 Mechanical drawing, dimensions in millimeters.

12 REFERENCES

Refer to TSPD's web site spdevices.com for the latest version of documents.

15-1494 Supported operating systems

18-2059 ADQUpdater user guide

20-2507 ADQ3 series development kit user guide

20-2521 ADQAssist user guide

21-2539 ADQ3 series user guide

22-2912 ADQ3 FWATD datasheet

22-2919 ADQ35-PDRX datasheet

23-3028 ADQ3 FWPD datasheet

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