ADQ35 Datasheet

The ADQ35 is a high-end 12-bit dual-channel data acquisition board optimized for use in high-throughput scientific applications. The ADQ35 features:

- **One analog channel at 10 GSPS**
- **Two analog channels at 5 GSPS per channel**
- **12 bits resolution**
- **14 GByte/s sustained data transfer rate to GPU**
- **14 GByte/s sustained data transfer rate to CPU**
- **Two external triggers**
- **General Purpose Input/Output (GPIO)**
- **Open FPGA for real-time signal processing**
- **Firmware option for averaging of records**
- **Firmware option for pulse analysis**
- **10-bit data compression for continuous streaming to GPU**

1 ORDERING INFORMATION

ADQ35 is available with a set of options listed in Table 1. Selection is done in three steps:

1. Select analog front-end configuration among related products.
2. Select the firmware options. The firmware FWDAQ is always included. Additional firmware options can be loaded into the board at any time.
3. Add additional features.

Table 1 Ordering information

Order code	Description	Datasheet	User guide
Related products: Hardware analog front-end options[1]			
ADQ35	DC-coupled front-end. This document.	**22-2918**	21-2539
ADQ35-PDRX	Built-in dual-gain front-end for pulse data	22-2919	21-2539
ADQ35-WB	AC-coupled wideband front-end for RF systems	20-2509	21-2539
Firmware options			
-FWDAQ	Included data acquisition firmware. This document.	**22-2918**	21-2539
-FWATD	Firmware advanced time domain. Add thresholding and waveform averaging in FPGA	22-2912	21-2539
-FWPD	Firmware pulse detection. Detect and analyze pulses in FPGA.	23-3028	21-2539
-FWOCT[2]	Firmware for Swept-Source OCT signal conditioning. K-space re-mapping, dispersion compensation, background subtraction, FFT	23-3019	23-3000
Additional features			
DEVDAQ[3]	Open FPGA for **FWDAQ**		20-2507
-W5Y	Extended warranty 5 years		

[1] The hardware options are factory installed and cannot be retrofit.
[2] Contact Teledyne SP Devices for information about availability.
[3] The development kit **DEVDAQ** opens the FPGA for the user to add custom functions. **DEVDAQ** is a one-time purchase. The FPGA bit files built from the design project using **DEVDAQ** can be used on any ADQ35 with a valid **FWDAQ** license.

2 ADQ35 INTRODUCTION

2.1 Features

- One and two analog input channels
- 10, 8 or 6 GSPS sampling rates in single channel mode
- 5, 4 or 3 GSPS sampling rate per channel in dual channel mode
- 12 bits resolution
- DC-coupled with 2.5 GHz bandwidth
- Programmable DC-offset
- Internal and external clock reference
- Clock reference output
- Internal and external triggers
- 8 Gbyte data memory
- 14 GByte/s sustained data streaming to CPU and GPU
- Data format 16-bit MSB aligned or rounded to 8-bit
- Compression to 10 or 12 bits for streaming to GPU
- Data interface PCIe Gen3 x16
- Averaging firmware FWATD
- Pulse analysis firmware FWPD
- Open FPGA enables custom firmware

2.2 Applications

- Swept-source optical coherence tomography (SS-OCT)
- Time-of-flight mass spectrometry
- Distributed optical fiber sensing
- LIDAR
- Scientific instruments
- Scanning acoustic microscopy

2.3 Advantages

- A space-saving, single-slot, high-performance digitizer supporting up to 55^{o}C ambient for demanding industrial applications
- Real-time processing and high data throughput
- Teledyne SP Devices' design services are available for fast integration to reduce time-to-market

2.4 System design optimization; open FPGA and streaming to CPU and GPU

High-performance data acquisition systems require high speed real-time analysis. ADQ35 offers a variety of options for efficient system design:

Streaming to GPU
ADQ35 supports up to 14 Gbyte/s sustained peer-to-peer streaming and streaming via pinned buffer to GPU. A GPU offers a powerful platform for implementing application-specific signal processing algorithms. Compressing the data to 10 bits allows continuous streaming to GPU for implementation of real-time algorithms.

Streaming to CPU
ADQ35 supports up to 14 GByte/s sustained streaming to host computer. Implementing the application-specific algorithms in the CPU results in an efficient system.

Open FPGA for real-time processing
ADQ35 offers an open FPGA for implementation of the application-specific computations in the FPGA. This gives the most compact system design. Firmware development kit is ordered separately.

Pulse data recording
The high sampling rate of ADQ35 makes it excellent for recording of fast pulses. The firmware options FWATD and FWPD includes efficient pulse processing in the FPGA.

For special use-cases, consider the related product ADQ35-PDRX, which offers a built-in dual-gain amplifier for pulse data capture with extended dynamic range. See datasheet 22-2919 for more details on the option ADQ35-PDRX.

RF systems
The ADQ35 offers a highly sensitive front-end with RF performance up to 2.5 GHz.

For higher frequencies, the related product ADQ35-WB provides an AC-coupled version of ADQ35 with up to 9 GHz useable analog bandwidth. See datasheet 20-2509 for more details on the option ADQ35-WB.

3 TECHNICAL DATA

Technical parameters are valid for ADQ35 operating with firmware FWDAQ. All parameters are typical unless otherwise noted.

Table 2 Analog input (front panel A and B)

Parameter	Condition	Min	Typical	Max	Unit
Basic parameters					
Bandwidth -3dB			2.5		GHz
Input range			0.5		Vpp
Input impedance			50		Ω
Coupling		DC			
Connector type		SMA			
Programmable DC-offset					
DC-offset range		-0.25		+0.25	V
Dynamic performance 2 channels mode at 5 GSPS					
Cross talk	< 2.5 GHz		-63		dB
Noise power density	0 to 2.5 GHz		-147		dBFS/√Hz
SNR	260 MHz, -1dBFS		52		dBc
SFDR	260 MHz, -1dBFS		63		dBc
ENOB relative full scale	10 MHz, -1dBFS		8.4		bits
ENOB relative full scale	260 MHz, -1dBFS		8.4		bits
ENOB relative full scale	810 MHz, -1dBFS		8.4		bits
ENOB relative full scale	1625MHz,-1dBFS		8.3		bits
Dynamic performance, 2 channels mode at 5 GSPS, FIR filter bandwidth 1.25 GHz[4]					
ENOB relative full scale	810 MHz, -1dBFS	bits	8.8		bits
Dynamic performance, 1 channel mode at 10 GSPS, connector A[5]					
Noise power density	0 to 5 GHz		-150		dBFS/√Hz
SNR	260 MHz, -1dBFS		51		dBc
SFDR	260 MHz, -1dBFS		61		dBc
ENOB relative full scale	10 MHz, -1dBFS		8.4		bits
ENOB relative full scale	260 MHz, -1dBFS		8.3		bits
ENOB relative full scale	810MHz,-1dBFS		8.3		bits
ENOB relative full scale	1625MHz,-1dBFS		8.2		bits
Dynamic performance, 1 channel mode at 10 GSPS, FIR filter bandwidth 2.5 GHz, connector A[5]					
ENOB relative full scale	260 MHz, -1dBFS		8.7		bits
ENOB relative full scale	810 MHz, -1dBFS		8.7		bits

[4] Built-in user-programmable digital FIR filter; symmetrical, 17 taps. Filter coefficients used for this test are [57, 92, –279, 21, 704, –720, –1163, 4127, 10784] / 2^{14}.

[5] Performance parameters are valid for 1 channel mode using input A. It is possible to use channel B as input but there are no parameters available for 1 channel mode using input connector B.

Table 3 Clock generator and front panel CLK connector

Parameter	Condition	Min	Typical	Max	Unit
Internal clock reference					
Frequency			10		MHz
Accuracy			±3 ±1/year		ppm
Internal sampling clock generator [6]					
Frequency range 1	2 channels		5000	5050[7]	MHz
Frequency range 2	2 channels		4000		MHz
Frequency range 3	2 channels		3000		MHz
Frequency range 1	1 channel		10000	10100[7]	MHz
Frequency range 2	1 channel		8000		MHz
Frequency range 3	1 channel		6000		MHz
External clock reference input (from front panel CLK connector) [8] [9]					
Frequency		0.4	10	500	MHz
Frequency [10]	Jitter cleaner enabled	10 -10 ppm	10	500 +10 ppm	MHz
Frequency	Delay line used		10	100	MHz
Delay line tuning range			500		ps
Signal level		0.5		3.3	Vpp
Input impedance	AC		50		Ω
Input impedance	DC		10k		Ω
Input impedance (high) [11]	AC		200		Ω
Connector type		SMA			
Clock reference output (on front panel CLK connector)[12]					
Frequency			10		MHz
Signal level	Into 50-Ω load		1.2		Vpp
Output impedance	AC		50		Ω
Output impedance	DC		10k		Ω

[6] The internal clock generator can generate frequencies in three different ranges.
[7] If the external clock reference deviates from its nominal value, the clock frequency can differ from expected. This is the maximum value where operation can be maintained.
[8] Clock reference from an external source to synchronize the ADQ35 to the external source.
[9] To minimize sampling clock jitter, the external reference should have as steep edges as possible. Therefore, a square wave with sharp edges is preferred over a sinewave, particularly at lower reference frequencies and amplitudes.
[10] The jitter cleaner requires the reference frequency to be a multiple of 10 MHz within ± 10ppm.
[11] Software-selectable high-impedance mode.
[12] The internal clock reference of the ADQ35 is made available to synchronize external equipment.

Table 4 Front panel TRIG connector

Parameter	Condition	Min	Typical	Max	Unit
Connector type			SMA		
Used as input (trigger or general-purpose input, GPI)					
Impedance	DC		50		Ω
Impedance (high) [13]	DC		500		Ω
Signal level	50-Ω mode	-0.5		3.3	V
Adjustable threshold	50-Ω mode	0		2.8	V
Signal level	High impedance	-0.5		5.5	V
Adjustable threshold	High impedance	0		2.3	V
Pulse repetition frequency	As trigger			10	MHz
Time resolution [14]	As trigger		50		ps
Update rate [14]	As GPI			156.25	MHz
Used as output (trigger or general-purpose output, GPO)					
Impedance	DC		50		Ω
Output level high VOH	Into 50-Ω load	1.8			V
Output level low VOL	Into 50-Ω load			0.1	V
Pulse repetition frequency				156.25	MHz

Table 5 Front panel SYNC connector (may be used as a trigger source with larger timing grid)

Parameter	Condition	Min	Typical	Max	Unit
Connector type			SMA		
Used as input (trigger or general-purpose input, GPI)					
Impedance	DC		50		Ω
Impedance (high) [13]	DC		500		Ω
Signal range	50-Ω mode	-0.5		3.3	V
Adjustable threshold	50-Ω mode	0		2.8	V
Signal level	High impedance	-0.5		5.5	V
Adjustable threshold	High impedance	0		2.3	V
Pulse repetition frequency	As trigger			10	MHz
Time resolution [14]	As trigger		3.2		ns
Update rate [14]	As GPI			156.25	MHz
Used as output (trigger or general-purpose output, GPO)					
Impedance	DC		50		Ω
Output level high VOH	Into 50-Ω load	1.8			V
Output level low VOL	Into 50-Ω load			0.1	V
Pulse repetition frequency				156.25	MHz

[13] Software-selectable high-impedance mode, suitable for source terminated signals.
[14] Timing properties are valid for 5 GSPS in 2 channel mode and 10 GSPS in 1 channel mode. Timing properties scale linearly with sampling frequency.

Table 6 Front panel GPIO connector (general purpose input/output)

Parameter	Condition	Min	Typical	Max	Unit
Connector type			SMA		
Used as input					
Impedance			50		Ω
Impedance (high) [15]			10		kΩ
Input level high VIH		2			V
Input level low VIL				0.8	V
Update rate [16]				156.25	MHz
Used as output					
Output Impedance			50		Ω
Output level high VOH	Into 50-Ω load	1.5			V
Output level high VOH	No load	3.2			V
Output level low VOL	Into 50-Ω load			0.1	V
Output level low VOL	No load			0.1	V
Update rate [16]				156.25	MHz

Table 7 Environmental and mechanical parameters

Parameter	Condition	Min	Typical	Max	Unit
Power and temperature					
Power consumption [17]	FWDAQ		48		W
Power supply		10.8	12	13.2	V
Operating temperature	FWDAQ[18]	0		55	°C
Operating temperature	FW options[19]	0		45	°C
Size					
Width 1 slot			18.42		mm
Length			269.55		mm
Height			111.15		mm
Weight			600		g
Compliances					
RoHS3		Yes			
CE		Yes			
FCC	Exclusion according to CFR 47, part 15, paragraph 15.103(c).				

[15] Software-selectable high-impedance mode, suitable for source terminated signals.
[16] Timing properties are valid for 5 GSPS in 2 channel mode and 10 GSPS in 1 channel mode. Timing properties scale linearly with sampling frequency.
[17] Power consumption depends on firmware option and use case. Power consumption is measured during acquisition and streaming of data at 14 Gbyte/s to PC.
[18] Operating the ADQ35 with FWDAQ and streaming data up to 14 Gbyte/s.
[19] Using firmware options from Teledyne SP Devices. Custom firmware designs may result in higher power consumption and thereby lower temperature range.

Table 8 Custom GPIO expansion. See section 10.

Parameter	Value
Connector type	40-pin FFC/FPC connector, pitch 0.5 mm
Number of differential input signals LVDS[20]	8
Number of single-ended 3.3-V LVCMOS I/O signals	5
Control bus	I2C, 3.3 V
Power supply	1.8 V, max 300 mA 3.3 V, max 1 A 5 V, max 600 mA

Table 9 Software support

Parameter	Value
Operating system[21]	Windows / Linux
GUI	Digitizer Studio
Example code	C, Python
API	C / C++
High-level API	LabVIEW / MATLAB / C#

Table 10 Data transfer[22]

Parameter	Value	Unit
Supported versions of data transfer standard PCIe	Gen1 / Gen2 / Gen3	
Supported number of lanes[23] [24]	1 / 4 / 8 / 16	
Sustained data rate to CPU / GPU	14	GByte/s
Sustained data rate peer-to-peer to GPU	14	GByte/s
Data format to CPU [25]	32 / 16 / 8	bits
Data format for streaming to GPU	32 / 16 / 12 / 10 / 8	bits

[20] The port can be set to output through the open FPGA development kit DEVDAQ.
[21] See 15-1494 Operating system support for a detailed listing of supported distributions.
[22] This is the data rate that the ADQ35 supports. Other parts of the system may limit the performance.
[23] The ADQ35 must be installed in a 16 lanes slot or a slot with a connector with an open end. If a shorter connector is used, the number of lanes and the maximum data rate is limited.
[24] PCIe bifurcation is required for 16 lanes.
[25] Default 16 bits MSB-aligned.

Table 11 Data acquisition

Parameter	Condition / Description	Min	Typical	Max	Unit
Rearm time[26]				20	ns
Acquisition memory (Data FIFO)	Shared by all channels		8		Gbyte
Record length	2-channel mode in steps of 1	2		2^{32}-1	samples
	1-channel mode in steps of 1	2		2^{32}-1	samples
Pre-trigger[27]	2-channel mode in steps of 16	0		16 336	samples
	1-channel mode in steps of 32	0		16 228	samples
Trigger delay[28]	2-channel mode in steps of 16	0		2^{36}-16	samples
	1-channel mode in steps of 32	0		2^{37}-32	samples
Trigger sources[29]	Start recording a set of data	External “TRIG”, “SYNC” and “GPIO” Logic OR of external sources Channel Logic OR of channels Internal generators Software			
Recording modes	Record length setting	Static (set by user) Dynamic (data controlled) Gated (trigger controlled) Continuous (unlimited)			
Timestamp reset	Reset or synchronize timestamp	External “TRIG”, “SYNC” and “GPIO” Software Internal periodic pulse generator			
Data format for streaming to GPU			32 / 16 / 12 / 10 / 8		bits

[26] Minimum time from the last sample of a record to the next trigger.
[27] Pre-trigger is set by assigning the parameter “horizontal offset” a negative value
[28] Trigger delay is set by assigning the parameter “horizontal offset” a positive value
[29] Trigger sources can be synchronized to clock reference for synchronous systems

4 FEATURES FOR DATA FLOW CONTROL, SYNCHRONIZATION AND PROCESSING

Table 12 Digital signal processing blocks

Object	Description
Digital Baseline Stabilizer (DBS)	Track and adjust the baseline to target level
Digital gain	Digital scaling of the signal
Digital offset	Add digital offset to signal
Digital FIR filter	User controlled 17 tap FIR filter
Sample skip	Skip samples after filtering to adjust sampling rate

Table 13 Pattern generators

Object	Description
Pattern generator	2 instances of general pattern generators
Periodic pulse generator	4 instances of periodic pulse generator

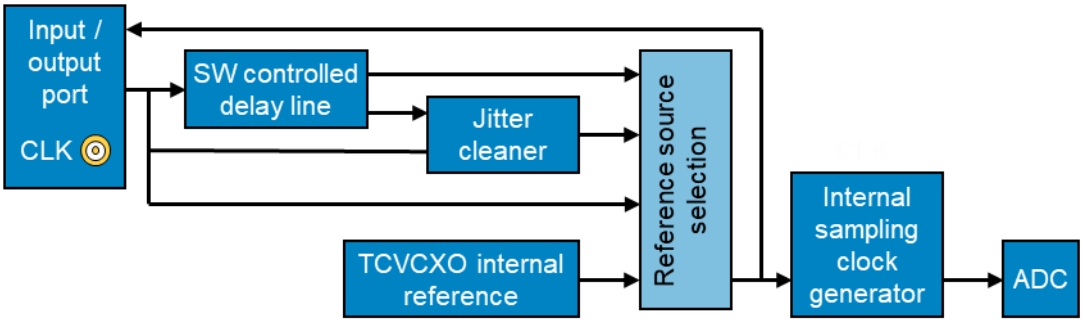

Figure 1 Clock generation block diagram.

Table 14 Clock generation

Function	Modes
Clock reference Phase and frequency reference for the clock system	Internal External through SMA connector CLK External with jitter cleaner and/or delay line
Sampling clock ADC sampling clock	Internal clock generator
Clock reference output	Internal clock reference (if selected as source)

5 FIRMWARE

5.1 FWDAQ

The FWDAQ is included with all digitizers. The firmware includes control of the hardware and recording of data.

The dual-gain channel combination included in FWDAQ requires a separate license for ADQ35.

5.2 FWATD

The FWATD is optional. It includes thresholding for noise suppression and accumulations of waveforms. See datasheet 22-2912 for more details.

The dual-gain channel combination included in FWATD requires a separate license for ADQ35.

5.3 FWPD

The FWPD is optional. It includes detection and analysis of pulses. See datasheet 23-3028 for more details.

The dual-gain channel combination is included in FWPD requires a separate license for ADQ35.

5.4 Managing firmware

The ADQ35 includes methods for managing different firmware options:

- The non-volatile memory on the digitizer can store up to four different firmware images, including the active firmware. The tool ADQAssist is used to change active image and to upload new images to the digitizer.
- Each hardware can include a license for multiple firmware images.
- If all firmware images of interest cannot be stored on the device, some may need be stored on the host computer for manual reprogramming via ADQAssist.
- The digitizer and the host computer must be power cycled to complete the switch of firmware image. This is required to let the PCIe bus enumerate with the new firmware.
- Some firmware features require a valid license key to activate. See the ordering information section **Error! Reference source not found.** for details about available firmware features.
- Switching mode between one channel at 10 GSPS and two channels at 5 GSPS requires switching the digitizer firmware image.

6 ABSLOUTE MAXIMUM RATINGS

Table 15 Absolute maximum ratings

Parameter	Condition	Min	Max	Unit
Power supply to GND		-0.4	14	V
Operating temperature[30]		0	55	°C
Storage temperature		-40	70	°C
Analog in		-2.5	+2.5	V
TRIG, SYNC in 50-Ω mode	Powered	-2	5	V
	Not powered	-2	2	V
TRIG, SYNC in 500-Ω mode	Powered	-2	6	V
	Not powered	-2	2	V
CLK REF	AC		5	Vpp
	DC	-5	5	V
GPIO	Powered	-1.5	5	V
	Not powered	-1.5	1.5	V
FFC / FPC differential signal to GND	Powered[31]	-0.5	2.3	V
	Not powered[31]	-0.5	0.5	V
FFC / FPC single-ended signal to GND	Powered[31]	-0.3	3.8	V
	Not powered[31]	-0.3	0.5	V

Exposure to conditions exceeding these ratings may reduce lifetime or permanently damage the digitizer. The digitizer with PCIe format has a built-in fan to cool the device. The built-in temperature monitoring unit will protect the digitizer from overheating by temporarily shutting down parts of the device in an overheat situation.
The SMA connectors have an expected lifetime of 500 operations. For frequent connecting and disconnecting of cables, connector savers are recommended.

[30] The absolute maximum temperature is the range where it is allowed to start the board.
[31] The absolute maximum ratings depend on whether the ADQ35 is powered or not. It is recommended to use the respective power rail in the FFC connector to power or enable the external drivers to avoid driving overvoltage into an unpowered digitizer. Use the 1.8 V rail for the differential signals and 3.3 V for the single-ended signals.

7 TYPICAL PERFORMANCE

7.1 Frequency response

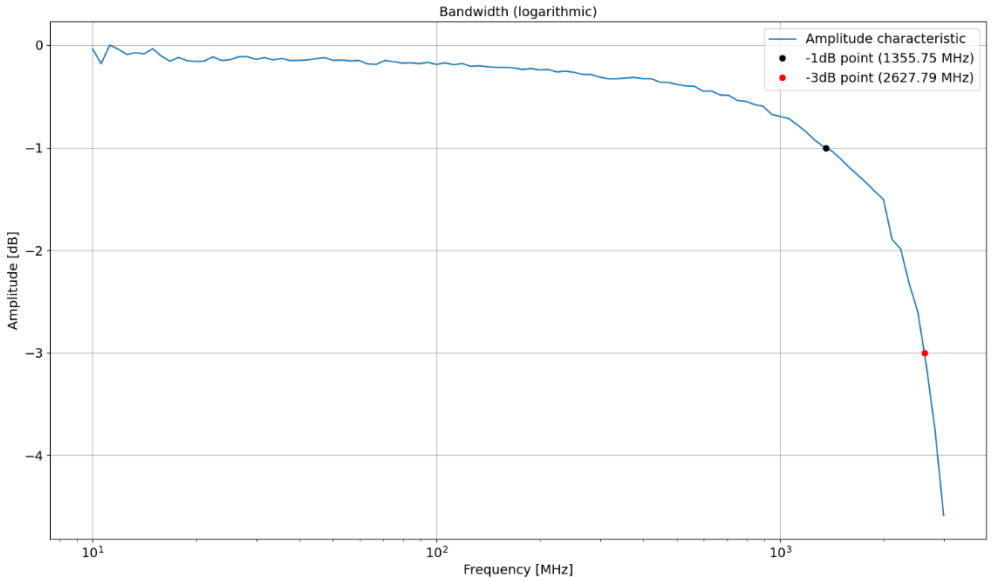

Figure 2 Frequency response, logarithmic frequency scale.

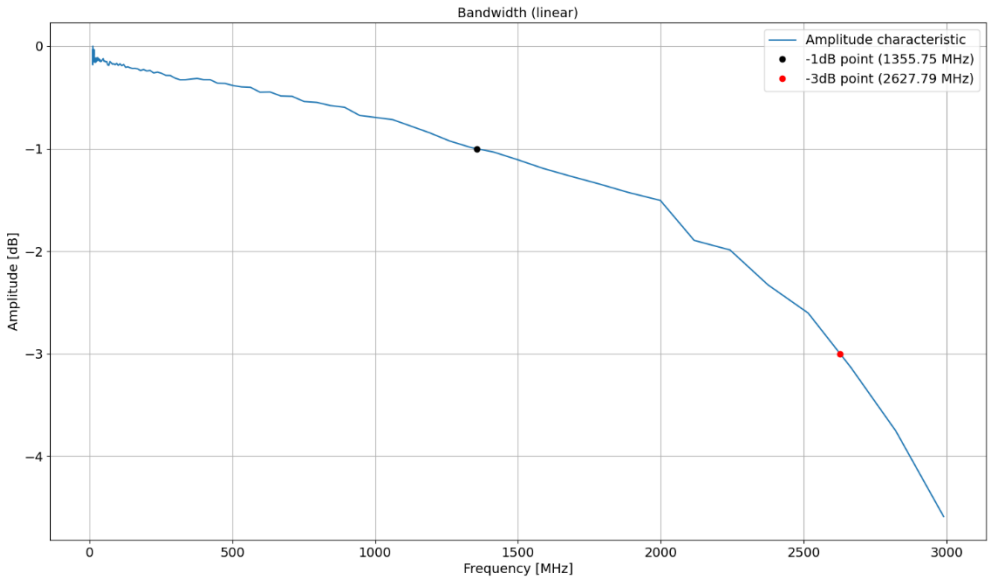

Figure 3 Frequency response, linear frequency scale.

7.2 FFT

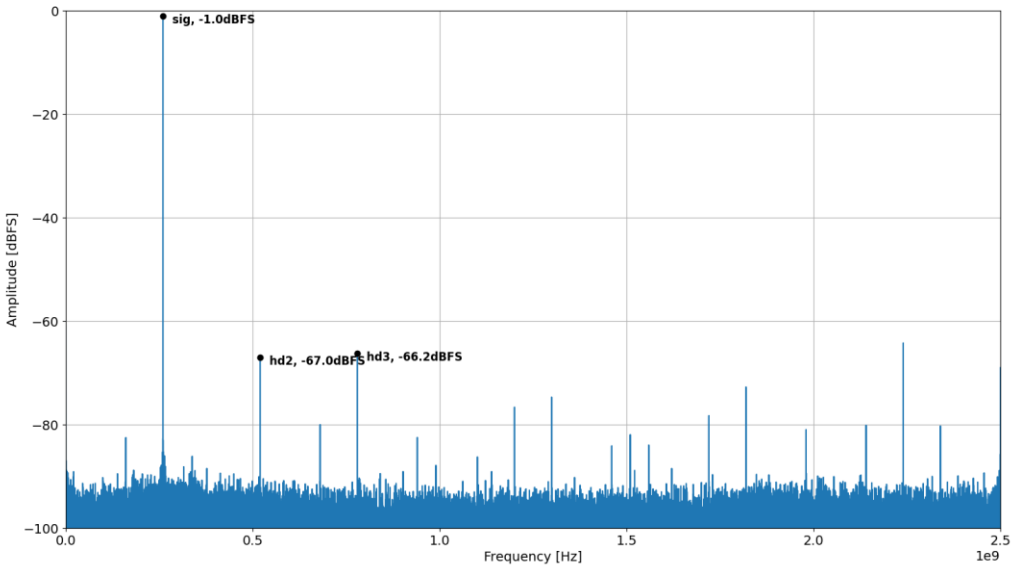

Figure 4 FFT typical performance 5 GSPS.

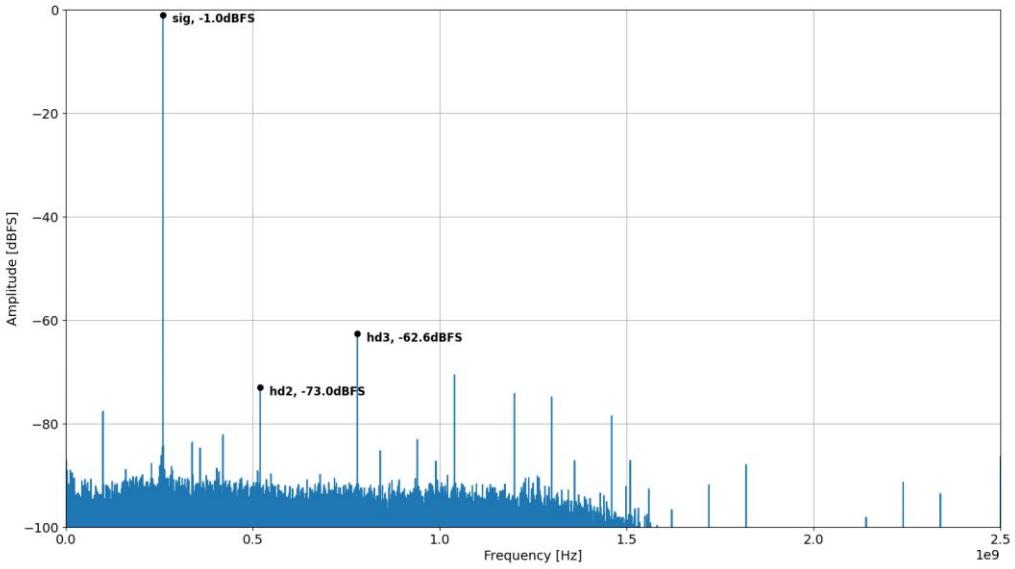

Figure 5 FFT typical performance 5 GSPS using FIR filter.

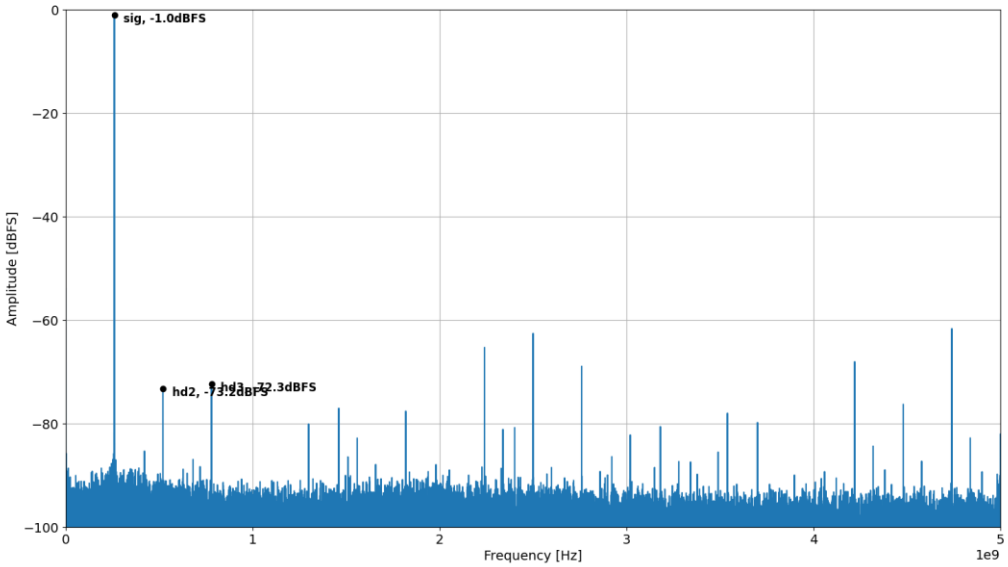

Figure 6 FFT typical performance at 10 GSPS.

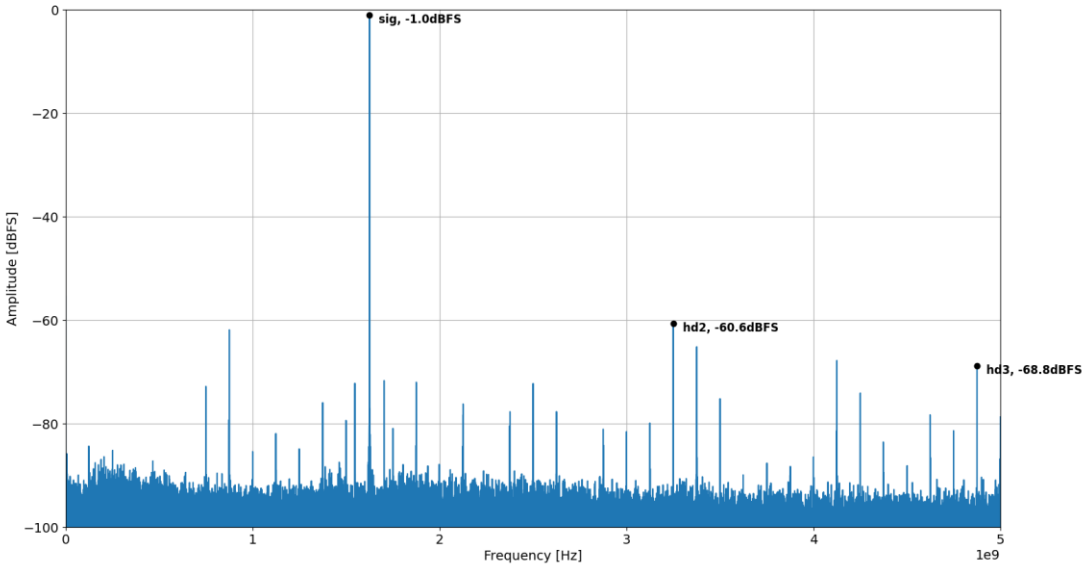

Figure 7 FFT typical performance 10 GSPS.

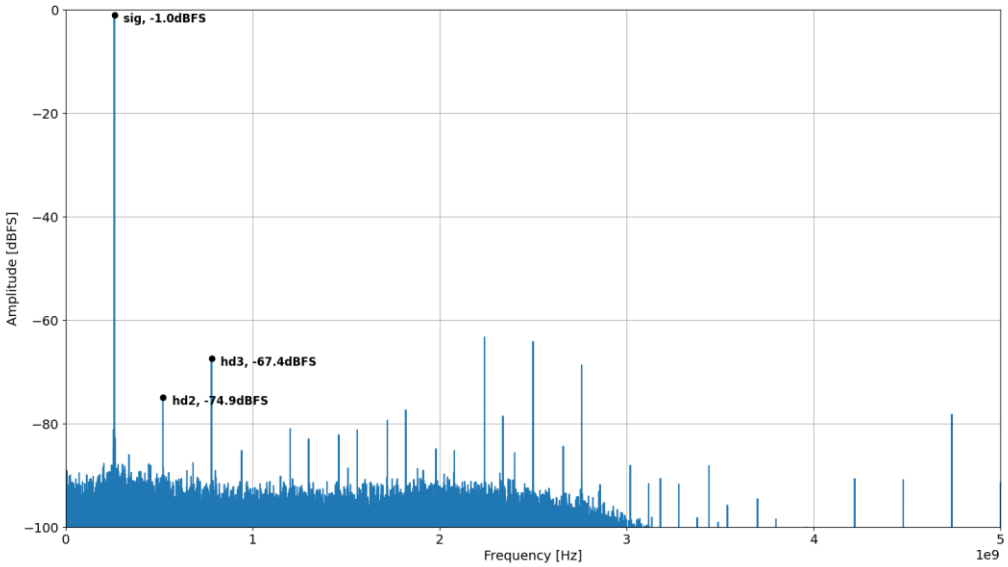

Figure 8 FFT typical performance 10 GSPS using FIR filter.

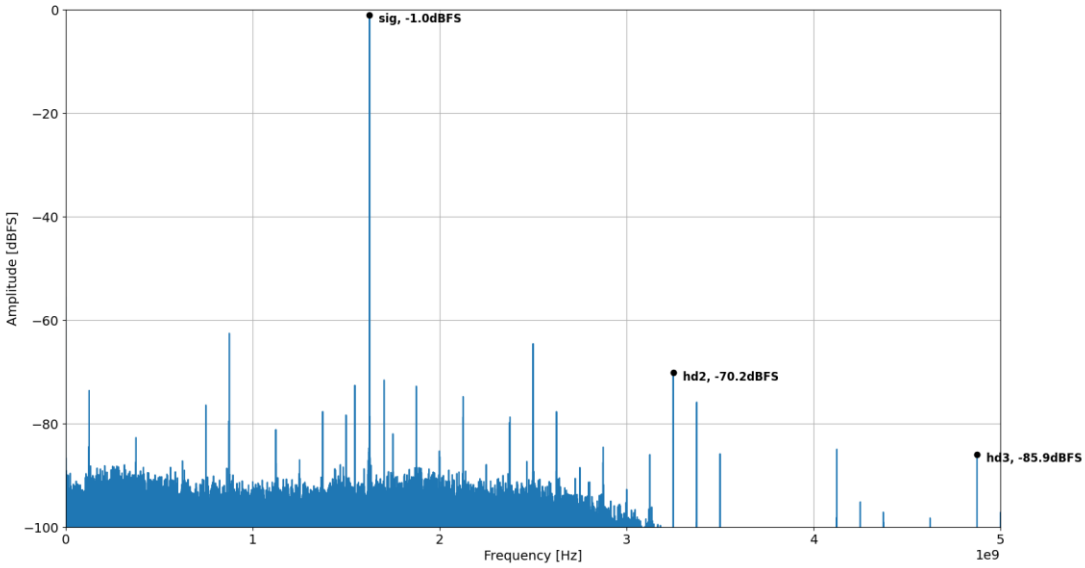

Figure 9 FFT typical performance 10 GSPS using FIR filter.

8 BLOCK DIAGRAM

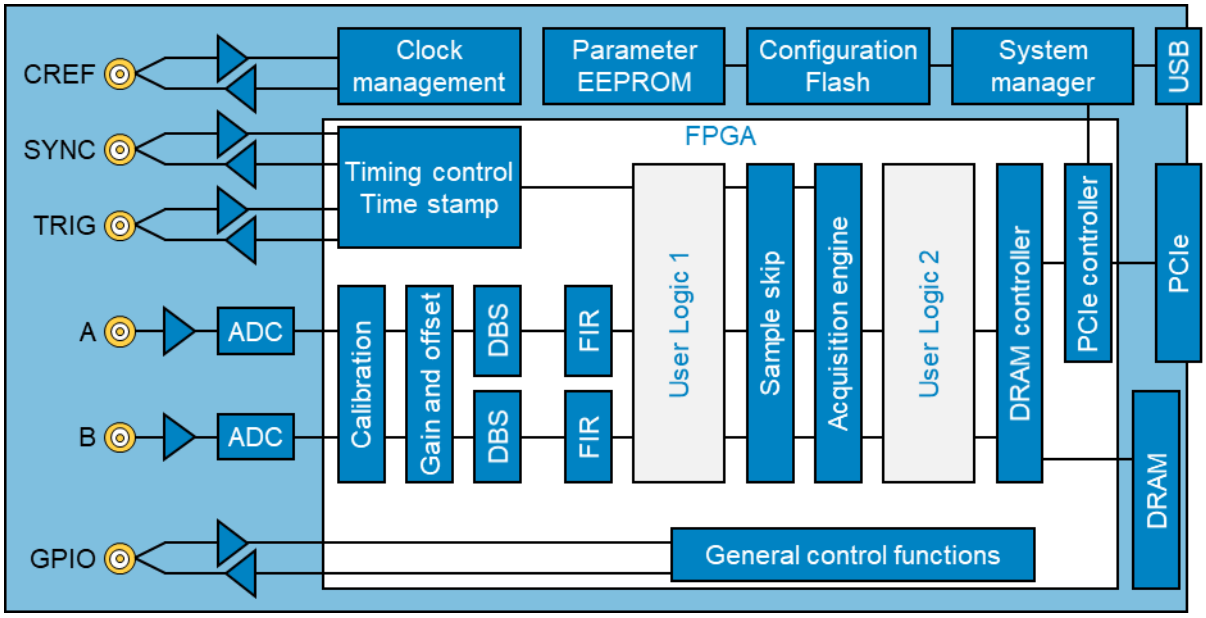

Figure 10 Block diagram.

Figure 10 shows a block diagram of ADQ35 in 2-channel mode. The boxes “User Logic” are available for custom real-time signal processing thought the firmware development kit (purchased separately).

9 HOST PC INTERFACE PCIE

The ADQ35-PCIe is powered from the power supply of the PC via a PCI Express 8-pin (2x4) auxiliary power supply connector. The connection in the cable should be as in Figure 11. It is also possible to operate the board from a PCI Express 6-pin (2x3) auxiliary power supply connector. Consider the power ratings for the respective connectors from the PC manufacturer.

It is important that the auxiliary power supply is turned on immediately when the PC starts. Otherwise, the digitizer will not be recognized on the PCI Express bus.

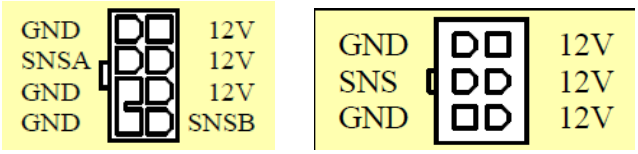

Figure 11 Power supply connection options. PCB connector.

10 GPIO EXPANSION

The FFC/FPC connector allows direct access to the FPGA for building custom expansion boards. The FCP connector requires custom firmware and is accessible through the FPGA development kit. The ADQ3 series user guide document number 21-2539 contains a description of connector.

Note that this connector is connected directly to the FPGA. Damage caused by custom hardware failure is not covered by warranty.

Contact Teledyne SP Devices' sales representative for more information.

11 MECHANICAL DRAWING

Figure 12 Photo of ADQ35.

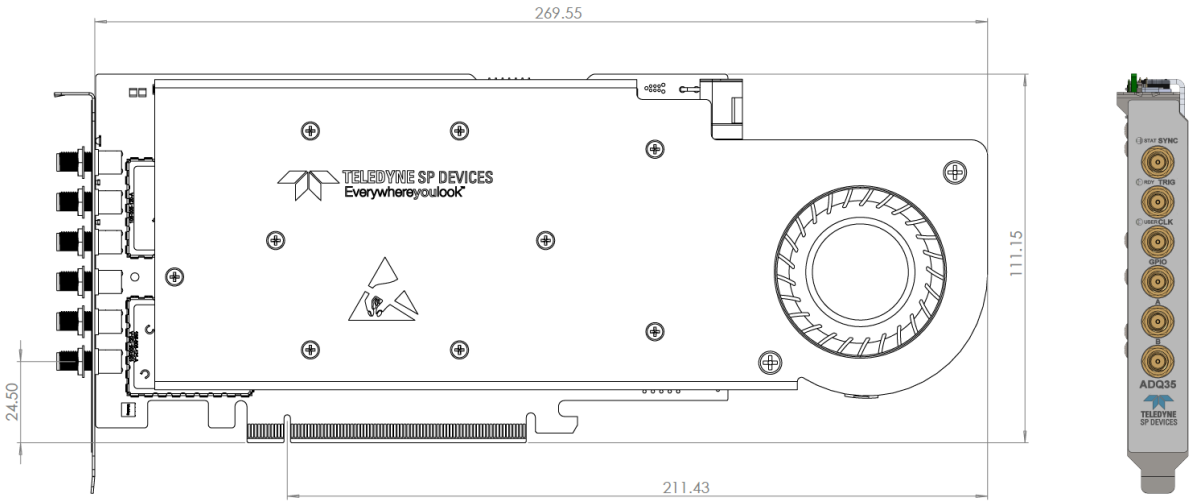

Figure 13 Mechanical drawing, dimensions in millimeters.

12 REFERENCES

Refer to Teledyne SP Devices' web site spdevices.com for the latest version of supplementary documents.

15-1494 Supported operating systems

18-2059 ADQUpdater user guide

20-2507 ADQ3 series development kit user guide

20-2509 ADQ35-WB datasheet

20-2521 ADQAssist user guide

21-2539 ADQ3 series user guide

22-2912 ADQ3 FWATD datasheet

22-2919 ADQ35-PDRX datasheet

23-3028 ADQ3 FWPD datasheet

Important Information

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