

# **Datasheet ADQ8-4X**



ADQ8-4X is a digitizer for modular instrumentation. ADQ8-4X is intended for large scale integration and features:

10 bits vertical resolution
4 and 2 analog channels
2 and 4 GSPS per channel
Multi-unit synchronization for large installations
Open FPGA for custom real-time applications (option)



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# **ADQ8-4X Datasheet**

#### Features

- 4 / 2 analog channels
- 2 / 4 GSPS sample rate per channel
- 10 bits vertical resolution
- Input impedance 50  $\Omega$
- DC-coupled
- 1 GHz analog bandwidth
- Digital filter for bandwidth control
- Programmable DC-offset
- High sensitivity input
- Vertical range setting 0.25 Vpp to 5 Vpp
- Over-voltage protection
- Internal clock reference
- Backplane clock reference
- Trigger time interpolation
- External trigger
- Multi-unit synchronization
- Timestamp for real-time operation
- 1 GBytes data memory
- 2.6 GBytes/s data streaming
- Available in PXIe form factor
- Digitizer Studio application software included
- Daisy chain multi-channel synchronization

# Applications

- Ultrasound applications
- Non-destructive testing
- Wireless communication
  - Time-of-flight
  - Scientific instruments
- · Particle physics
- Thomson scattering
- Semiconductor test
- ATE
- Test and measurement
- Quantum technology

#### Advantages

- Host PC interface options and large scale integration support for optimized systems partitioning.
- Advanced analog front-end and high sample rate for meeting detector and measurement requirements.
- Application specific firmware options and realtime custom processing solutions for advanced systems for optimized cost of ownership.
- SP Devices' design services are available for fast integration to lower the time-to-market.

#### ORDER CODE NAME DESCRIPTION Full flexible analog front-Flexible analog front-end including user controlled DC-offset, and $-VG^1$ end voltage range -PXIE Form factor for integration in a PXI Express 3U chassis PXI Express format Form factor for integration in a MTCA.4 chassis. MTCA.4 format -MTCA<sup>2</sup> Data acquisition firmware Data acquisition functions for 4 channels, 2 GSPS -FWDAQ2G<sup>3</sup> Data acquisition firmware Data acquisition functions for 2 channels, 4GSPS -FWDAQ4G<sup>4</sup> Firmware development kit Open the FPGA to add custom firmware to -DEV8DAQ<sup>5</sup> -FWDAQ2G and -FWDAQ4G -W5Y Warranty 5 years Warranty extended from 3 to 5 years<sup>6 7</sup>

1. Always included with the ADQ8-4X. Availability of ADQ8-4X without –VG option installed is to be confirmed. Please contact a TSPD sales representative for more information.

2. Availability is to be confirmed. Please contact a TSPD sales representative for more information.

- 3. Always included with the ADQ8-4X.
- 4. Always included with the ADQ8-4X.
- 5. Purchased separately. Development kit for -FWDAQ2G and -FWDAQ4G included.
- 6. Included warranty is 3 years from the date the product is shipped by Teledyne SP Devices. This option extends the warranty to 5 years from the date the product is shipped by Teledyne SP Devices.
- 7. Warranty extension must be ordered before included 3 years warranty is expired.

## Options summary



# 1 Technical data

All values are typical unless otherwise noted.

All parameters are valid for and limited to firmware -FWDAQ2G unless otherwise noted.

Table 1:	Analog input with –VG option installed. Typical parameters.
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PARAMETER		-VG-FWDAQ2G	–VG–FWDAQ4G
Analog inputs			
Connector		SN	ЛА
Coupling		D	С
Input range settings	[V <sub>pp</sub> ]	0.2	
		0.	
		2.	5
			5
Variable DC-offset	[V]	± 0.5 *	range <sup>1</sup>
Cross talk isolation DC – 500 MHz	[MHz]	> 60	) dB
Over-voltage protection		See Ta	able 11
Input impedance	[Ω]	50 ±	3 %
Idle channel noise (Range 0.25)	[dBFS / Hz]	-135.8	-138.8
Idle channel noise (Range 0.5 1 2.5 5)	[dBFS / Hz]	-141.8	-144.8
Flatness –1 dB	[MHz]	300	300
Bandwidth upper limit –3 dB	[MHz]	1000	1000
Analog performance. Test signal at –1	dBFS up to 40	2 MHz.	
SNR (Range 0.25 V <sub>pp</sub> )	[dBFS]	46	46
SNR (Range 0.5 1 2.5 5 V <sub>pp</sub> )	[dBFS]	51	51
SFDR <sup>2</sup> (All ranges)	[dBFS]	64	64
SFDR <sup>3</sup> (All ranges)	[dBFS]	_	57
ENOB (Range 0.25 V <sub>pp</sub> )	[bits]	7.4	7.4
ENOB (Range 0.5 1 2.5 5 V <sub>pp</sub> )	[bits]	8.0	8.0

1. Rail-to-rail on all input range settings.

2. Not including Interleaving tone

3. Interleaving tone included



#### Table 2: Clock

PARAMETER		–FWDAQ2G	–FWDAQ4G
Internal Clock Reference			
Frequency	[MHz]	10 ± 3 ppm	10 ± 3 ppm
Drift		± 1 ppm / year	± 1 ppm / year
PXIe backplane clock reference			
PXIe sync	[MHz]	10	10
PXIe clock	[MHz]	100	100
Backplane clock reference accuracy		± 10 ppm	± 10 ppm
External clock reference			
Frequency	[MHz]	10	10
Clock reference output			
Frequency	[MHz]	10	10
External clock			
Clock frequency	[MHz]	1000 ( <sup>1</sup> )	1000 ( <sup>2</sup> )
Sample skip			
Ratio <sup>3</sup>		1 2 4 8 10 12 14 2 <sup>16</sup>	1 2 4 8 10 12 14 2 <sup>16</sup>
Front panel connector clock input	·		
Signal level minimum	[Vpp]	0.2	0.2
Signal level recommended	[Vpp]	0.6	0.6
Signal level maximum	[Vpp]	0.8	0.8
Input impedance AC	[Ω]	50	50
Input impedance DC	[Ω]	10 k	10 k
Connector		SMA	SMA <sup>4</sup>
Front panel connector clock output			
Level (into 50 Ω, typical)	[V]	1.6	1.6
Output impedance AC	[Ω]	50	50
Output impedance DC	[Ω]	10 k	10 k
Coupling		AC	AC
Connector		MCX	MCX

1. The external clock frequency of 1 GHz result in a sampling rate of 2 GSPS.

The external clock frequency of 1 GHz result in a sampling rate of 4 GSPS.
 Sample skip ratio of 200 means that the data rate is reduced a factor of 200, that is from 1 GSPS to 5 MSPS.

4. Connector is shared between input and output. The direction is software controlled.



#### Table 3: Trigger

PARAMETER		ADQ8-4X–VG–PXIE
Analog channel as trigger <sup>1</sup>		
Connector		SMA
Impedance DC	[Ω]	see Table 1
Signal level <sup>2</sup>	[V]	see Table 1
Signal swing	[Vpp]	see Table 1
Adjustable software controlled trigger threshold <sup>3</sup>	[V]	see Table 1
Time resolution (interpolated value)	[ps]	25
Jitter RMS	[ps]	10
Star B backplane trigger		
Connector		Backplane
Time resolution	[ns]	4
External trigger input on front panel		
Connector (shared with output)		SMA
Time resolution	[ns]	1
Adjustable threshold	[V]	0 to +3.0
Signal level	[V]	–0.5 to +3.3
Input impedance	[Ω]	50
Input impedance high <sup>4</sup>	[Ω]	500
External trigger output on front panel		
Connector (shared with input)		SMA
Level (no load, typical)	[V]	0 to +3.3
Output impedance	[Ω]	50

1. Use one of the analog inputs as trigger. The timing of the trigger is interpolated to high accuracy.

2. Use the DC-offset and range settings to adjust to the trigger signal. See Table 1 for details.

3. The setting of the threshold is within the signal range selected.

4. Software controlled high impedance for bussed connection.

#### Table 4: SYNC trigger signal

		ADQ8-4X–VG–PXIE
Output		
Connector		MCX
Impedance DC	[Ω]	50
Signal level output (no load)	[V]	0 to 3.3
Input		
Connector		MCX
Impedance DC <sup>1</sup>	[Ω]	10 k
Vil_max	[V]	0.8
Vih_min	[V]	2.0
Input synchronous mode <sup>2</sup>		
Time resolution	[ns]	100
Input asynchronous mode		
Time resolution	[ns]	4
Jitter asynchronous mode RMS	[ns]	1.15

1. The signal has to be source terminated with 50  $\Omega.$ 

2. Synchronous mode phase locked to 10 MHz reference.



#### Table 5: General specifications

		ADQ8-4X–VG–PXIE	
Key parameters			
Channels (–FWDAQ2G)		4	
Sample rate / channel (–FWDAQ2G)	[GSPS]	2	
Channels (–FWDAQ4G)		2	
Sample rate / channel (–FWDAQ4G)	[GSPS]	4	
Resolution	[bits]	10	
Data memory <sup>1</sup>	[GByte]	1	
Firmware function			
Trigger modes		Channel, External, Backplane Star B, Software	
Clock reference		Internal, External, Backplane	
Acquisition modes		Multi-record, streaming	
Synchronization		Daisy-chain trigger, trigger time interpolation	
Mechanical			
Weight	[g]	520	
Board width including –VG	[slot]	2	
Board height		3U	
Electrical			
Power supply	[V]	12	
Power dissipation	[W]	46	
Temperature range			
Ambient operating	[°C]	0 to 45 <sup>2</sup>	
Storage	[°C]	–40 to 70	
Compliances			
CE		$\checkmark$	
RoHS3		$\checkmark$	
FCC		Exclusion according to CFR 47, part 15, paragraph 15.103(c)	

1. The data memory is shared between data from all channels.

2. High fan setting required if available on the chassis. Blocking airflow through empty slots is recommended and may be necessary.

#### Table 6: Data acquisition parameters –FWDAQ2G: Multi-record

		STEP SIZE	MIN / MAX
Rearm time	[us]	-	4
Pre-trigger length	[samples]	1	0 to record length
Trigger delay	[samples]	8	0 to 2 <sup>32</sup> –8
Record length	[samples]	1	8 to 100 M
Data transfer speed max	[GBytes/s]	-	3.2
Data transfer speed sustained	[GSamples/s]	-	1.3
Data memory	[samples per channel]	-	100 M



### Table 7: Data acquisition parameters –FWDAQ2G: Streaming<sup>1</sup>

		STEP SIZE	MIN / MAX
Rearm time	[ns]	-	max 168
Pre-trigger length	[samples]	8	0 to 16 k
Trigger delay	[samples]	8	0 to 2 <sup>32</sup> –8
Record length	[samples]	8	8 to 100 M
Data transfer speed max	[GBytes/s]	-	3.2
Data transfer speed sustained	[GSamples/s]	-	1.3
Data memory	[samples per channel]	-	100 M

1. See 20-2465 on streaming interface

#### Table 8: Data acquisition parameters –FWDAQ4G: Multi-record

		STEP SIZE	MIN / MAX
Rearm time	[us]	-	4
Pre-trigger length	[samples]	1	0 to record length
Trigger delay	[samples]	16	0 to 2 <sup>32</sup> –16
Record length	[samples]	1	8 to 200 M
Data transfer speed max	[GBytes/s]	-	3.2
Data transfer speed sustained	[GSamples/s]	-	1.3
Data memory	[samples per channel]	-	100 M

# Table 9: Data acquisition parameters –FWDAQ4G: streaming<sup>1</sup>

		STEP SIZE	MIN / MAX
Rearm time	[ns]	-	max 168
Pre-trigger length	[samples]	16	0 to 16 k
Trigger delay	[samples]	16	0 to 2 <sup>32</sup> –16
Record length	[samples]	16	8 to 200 M
Data transfer speed max	[GBytes/s]	-	3.2
Data transfer speed sustained	[GSamples/s]	-	1.3
Data memory	[samples per channel]	_	100 M

1. See 20-2465 on streaming interface

### Table 10: Software support

	COMMENT			
Operating systems <sup>1</sup>				
Windows 8 / 8.1, 32-bit and 64-bit	$\checkmark$			
Windows 10, 32-bit and 64-bit	√			
Linux	4			
Application				
C/C++	API, examples			
Python	Example scripts			
Digitizer Studio	Application tool			

1. See "15-1494 Operating System Support" for supported distributions.



# 2 Spectral response

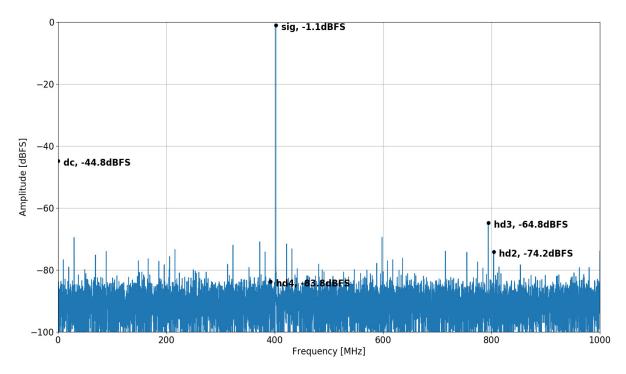


Figure 1: ADQ8-4X–VG–FWDAQ2G spectral performance at –1 dBFS, range 0.5 Vpp.

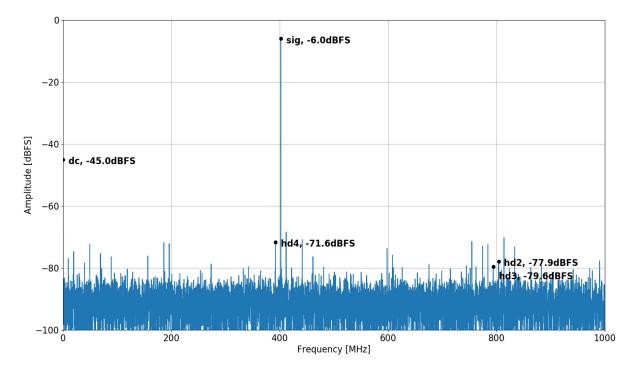


Figure 2: ADQ8-4X–VG–PXIE spectral performance at –6 dBFS, range 0.5 Vpp.



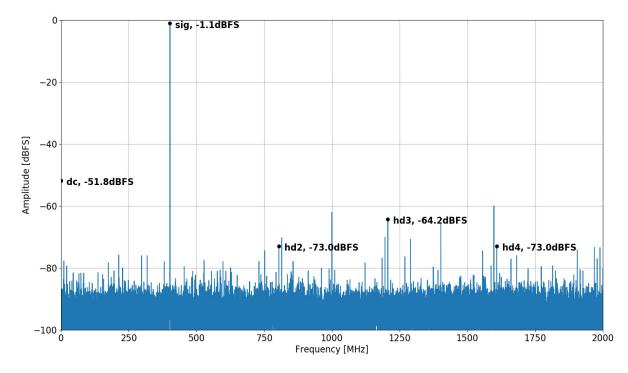


Figure 3: ADQ8-4X–VG–FWDAQ4G spectral performance at –1 dBFS, range 0.5 Vpp.

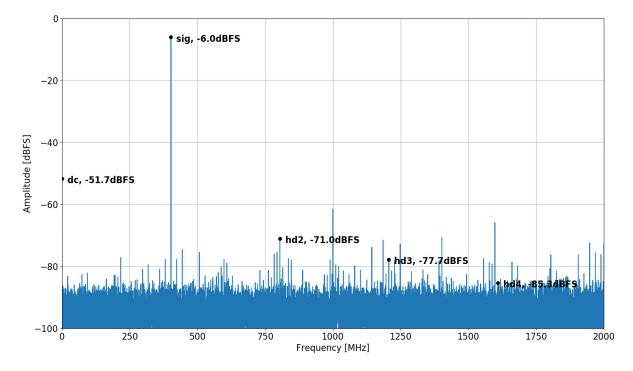


Figure 4: ADQ8-4X–VG–FWDAQ4G spectral performance at –6 dBFS, range 0.5 Vpp.



# 3 Frequency response

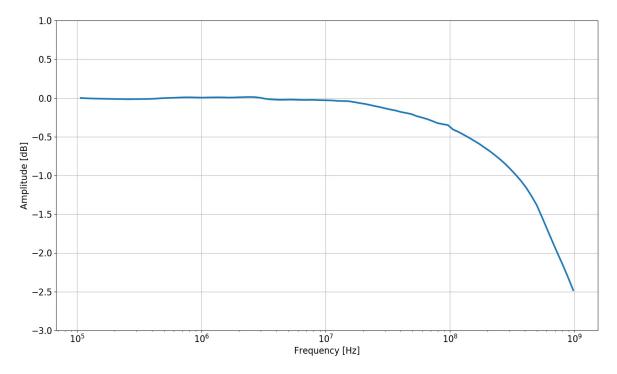


Figure 5: ADQ8-4X–VG, –FWDAQ2G and –FWDAQ4G frequency response.



# 4 Absolute maximum ratings

Stresses beyond conditions listed under Absolute Maximum Ratings **Table 11** may cause permanent damage to the device. The analog inputs are protected from over-voltage but the values in **Table 11** must never be exceeded. Built-in temperature monitoring protects the ADQ8-4X from overheating shutting down parts of the device in an overheat situation.

#### Table 11: Absolute Maximum Ratings

PARAMETER		MIN	MAX
Analog input <sup>1</sup>			
Voltage to GND	[V]	- 5.0	+ 5.0
Trigger			
Voltage to GND	[V]	-2.3	5.0
SYNC			
Voltage to GND	[V]	-0.3	+3.6
CLKIN			
Voltage to GND	[V]	-5.0	+5.0
Power supply			
Voltage to GND	[V]	-0.4	14
Temperature			
Ambient operating	[°C]	0	45

1. Also valid for analog channel used as trigger.



# 5 Block diagram

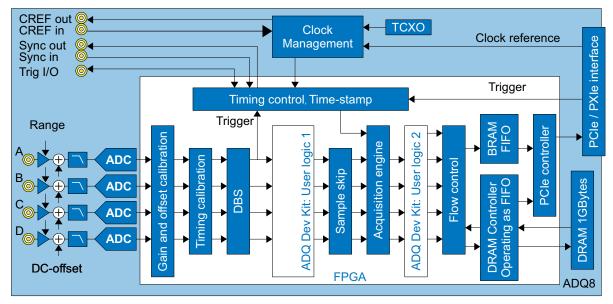
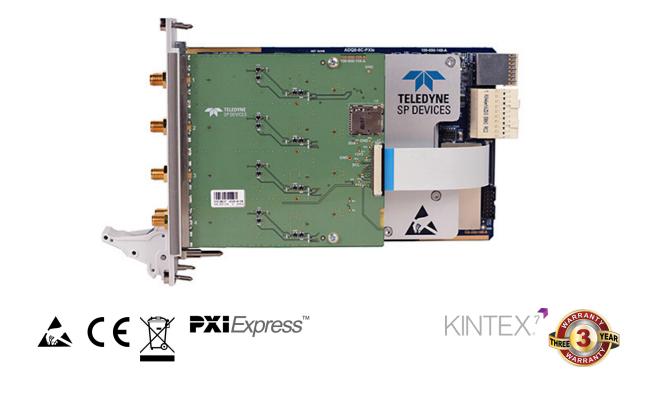


Figure 6: Block diagram for ADQ8-4X





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