ADQ7-FW2DDC firmware datasheet

ADQ7-FW2DDC: application-specific firmware including digital down-converters for radio applications:

- *Digital Down Conversion*
- *Decimation*
- *Streaming data*
- *Multi-channel synchronization*
- *Differential / single-ended input*
- *Two analog inputs*
- *Two digital radio channels*
- *Option with open FPGA.*

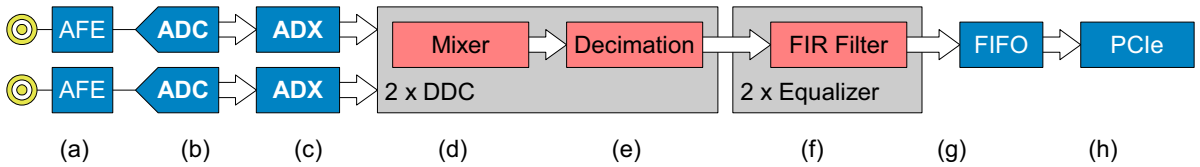
Applications:

- *RF system*
- *Channel sounder*
- *RF recording*
- *Satellite monitoring*
- *Radar*
- *Semiconductor RF test*
- *Spectrum monitoring*
- *Test and measurement*
- *RF production test*
- *5G*

1 Block diagram

The purpose of the ADQ7-FW2DDC firmware option is to implement an efficient radio receiver for a general purpose radio architecture. The structure of the ADQ7-FW2DDC is shown in **Figure 1**.

In order to achieve high bandwidth, ADQ7-FW2DDC benefits from SP Devices' powerful interleaving technology ADX. ADX removes typical interleaving artifacts. The result is a unique instantaneous bandwidth of up to 2.5 GHz with high linearity.



#	DESCRIPTION	REF
a	There are two analog inputs for receiving either, I and Q, two RF channels, or a differential RF signal. The analog front-end is either DC- or AC-coupled.	**Table 1**
b	The high performance A/D converters are interleaved to reach higher instantaneous bandwidth.	**Table 1**
c	ADX is SP Devices proprietary IP for interleaving correction of A/D converters which enable the unique wide band performance of ADQ7.	**Table 2**
d	The quadrature mixer transforms the center frequency of the RF signal to the pass-band of the decimation filters.	**Table 3**
e	The decimation reduces the sample frequency and increase SNR in the signal band.	**Table 4**
f	This user-defined filter reduces the bandwidth and the noise level. The filter can also implement an equalizer or IQ balance.	**Table 5**
g	The FIFO handles the transfer of data from the real-time data acquisition to the PC.	
h	The connection to the host PC is using PCIe standard for both PCIe and PXIe systems.	

Figure 1: Principle of the ADQ7-FW2DDC.

2 Technical data

All values are typical unless otherwise noted.

Table 1: General parameters

		ADQ7-FW2DDC
Key parameters		
Analog input channels		2
Digital output channels		2
Digital signal representation low decimation factor	[bits]	16, 32
Digital signal representation high decimation factor	[bits]	32
Firmware input bandwidth	[GHz]	5
Firmware output bandwidth max	[GHz]	5
Sustained streaming bandwidth	[GHz]	1

Table 2: ADX parameters

		ADQ7-FW2DDC
Time interleaving spur level up to 5 GHz	[dBFS]	–60

Table 3: NCO parameters

		ADQ7-FW2DDC
Frequency resolution[1]	[Hz]	1.1642
Spur level	[dBFS]	–95

1. Computed as (sampling rate / 2) / 2^{31}.

Table 4: Decimation parameters

		ADQ7-FW2DDC
DDC 1 and 2[1]		
Minimum decimation factor		2^0
Maximum decimation factor		2^{34}
Pass band ripple	[dB]	0.01
Stop band attenuation	[dB]	80
Bandwidth, pass band		80 %

1. Example: The input to the DDC is at 5 GSPS and a Nyquist bandwidth of 2.5 GHz. A decimation of 2^3 = 8 times means that the output from the DDC is 0.625 GSPS and a Nyquist bandwidth of 0.3125 GHz. The pass band (80%) is then 0.25 GHz.

Table 5: Equalizer parameters

		ADQ7-FW2DDC
Filter length	[taps]	5
Maximum filter coefficient		$2–2^{14}$
Minimum filter coefficient		–2
Filter coefficient length	[bits]	16
Input data word length maximum	[bits]	25

3 Related products

The ADQ FPGA Development Kit for ADQ7-FW2DDC opens the FPGA for the user to include custom real-time signal processing. The ADQ FPGA Development Kit is purchased separately. Please contact a Teledyne SP Devices sales representative for information about availability.

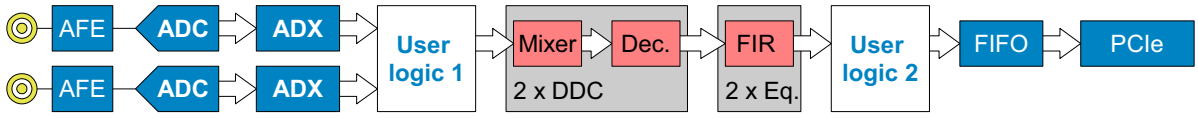


Figure 2: ADQ7-FW2DDC with User Logic 1 and User logic 2 for ADQ Development Kit.

4 Compatible hardware

ADQ7-FW2DDC is compatible with

- ADQ7WB-PXIe
- ADQ7WB-PCIe
- ADQ7DC-PXIe in dual channel mode
- ADQ7DC-PCIe in dual channel mode
- ADQ7DC-USB in dual channel mode

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