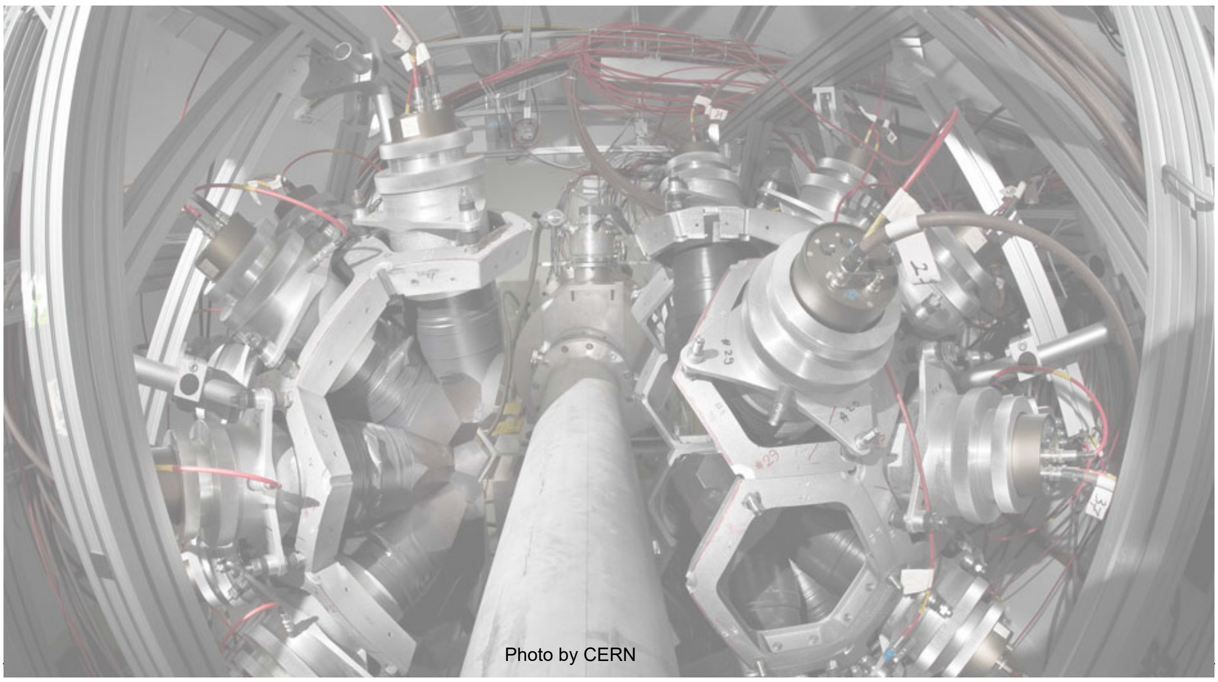
ADQ7DC–FWPD Datasheet

The pulse detection firmware option –FWPD equips ADQ7DC with sophisticated tools to identify, analyze, and collect pulsed data streams in real-time.



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ADQ7DC–FWPD Datasheet

Features

- High performance data acquisition
- 1 / 2 analog channels
- 10 / 5 GSPS per channel
- 14 bits vertical resolution
- Synchronization support
    - External trigger
    - Internal trigger output
    - Software trigger
    - Multi-unit synchronization
- Pulse organization tools
    - Detection window to select pulses
    - Automatic pulse detection
    - Per-channel individual level trigger
- Data management
    - Adaptive record length for zero suppression and optimal memory usage
    - Real-time pulse analysis in FPGA
    - Custom pulse analysis enabled through ADQ7DC Development Kit
    - Padding to ensure a minimum level of activity
    - Dynamic data transfer of raw data and analysis data

Applications

- Big Physics
- Time-of-flight
- Scientific instruments
- LIDAR
- RADAR
- Neutron time-of-flight

–FWPD package includes support ADQ7DC in
2 channels mode at 5 GSPS
1 channel mode at 10GSPS

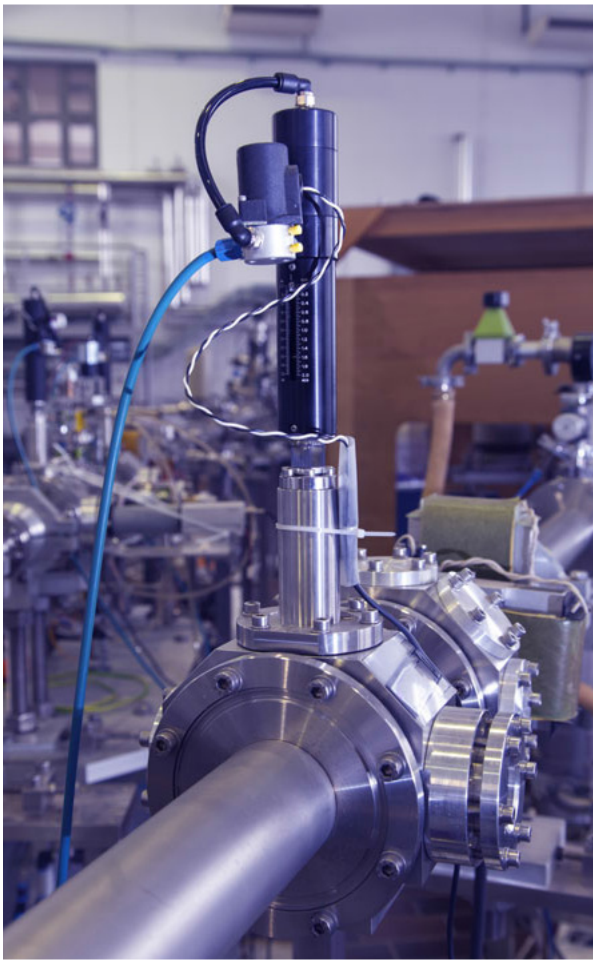
–FWPD package includes support for interfaces:

PCIe	USB3.0
cPCIe / PXIe	Micro-TCA.4

Mark order with “10GBE” to include support for 10GbE optical interface.

Advantages

- Advanced analog front-end, trigger functions, and high sampling rates for meeting systems requirements.
- Efficient utilization of dynamic range with an optional DC-offset.
- Highly accurate and stable baseline for pulse detection applications.
- Data multiplexing allows for raw data and pulse analysis metadata to be output simultaneously from the same channel.
- Teledyne SP Devices’ design services are available for fast integration to lower time-to-market.



Functional summary

The purpose of the firmware option –FWPD is to analyze pulse data and limit the acquired data to the interesting regions and parameters. The firmware can detect pulses and adapt the data capture to the properties of the pulses.

Figure 1 shows a high-level block diagram of the firmware. The firmware consists of two parts; pulse identification and pulse analysis. The pulse identification tracks the baseline and identifies when pulses begin and end. The recording includes dynamic record length which suppresses zeros, that is, parts of the signal below threshold are discarded and disk space is saved.

The pulse analysis finds the peak value and the width of a pulse. These real-time calculations are performed in the FPGA. Custom pulse analysis is enabled through the ADQ7DC Development Kit which opens the FPGA for the user. ADQ7DC Development Kit is purchased separately.

Software support

The –FWPD option is supported by Windows and a number of Linux distributions. For a detailed list of operating systems, see document 15-1494. The software development kit (SDK) contains the ADQAPI, drivers, examples and documentation.

The recommended programming environment for high performance is C/C++. Python example code is also available.

Note that there is *NO* support for MATLAB, LabVIEW, nor ADCaptureLab.

Ordering information

The –FWPD option can either be ordered together with an ADQ7DC, or separately, for updating an existing unit. When ordered separately, the serial number of the ADQ7DC has to be provided to get a license key for activating the firmware.

Order ADQ Development Kit for –FWPD separately. Note that the development kit is tied to a digitizer model and a firmware option.

Acquisition	High resolution (14 bits) and high speed (10 GSPS) recording with the ADQ7DC digitizer.	High performance recording
DBS	Stabilize the baseline with Teledyne SP Devices' proprietary algorithm Digital baseline stabilizer (DBS).	Reliable reference
Detection window	Define the timing window where pulses are accepted.	Frame the pulses
Peak detection	Detect the pulse and calculate leading and trailing edges.	Detect the pulses
Peak analysis	Analyze the peak in real-time. The analysis includes peak value, pulse width (time-over-threshold). Custom analysis is available through ADQ7 Development Kit.	Pulse data
Time stamp	Get timing information for detection window and individual pulses.	Pulse timing
Latency control	Control latency to get a minimum throughput by padding with dummy data (**Figure 3**).	Flow control
Data formating	Make records of the data to be sent to host (**Figure 3**).	Data transfer management

Figure 1: Block diagram of the main functionality of –FWPD.

Technical data

Note that the 14-bit ADQ7DC digitizer uses an MSB-aligned 16-bit data representation. The digital signal processing, for example DBS, will affect the two LSBs making them non-zero. For the general specification of the ADQ7DC digitizer, please refer to the ADQ7DC datasheet (17-2017).

Table 1 presents the specification. There are two separate sets of data, one for dual channel mode at 5 GSPS and one for single channel mode at 10 GSPS.

Table 2 presents definitions and acronyms.

Table 1: Specification of FWPD

		2 CHANNELS MIN	2 CHANNELS MAX	1 CHANNEL MIN	1 CHANNEL MAX
Thresholds [1]					
Analog DC-offset level [2]	[codes]	-2^{15}	$+2^{15}-1$	-2^{15}	$+2^{15}-1$
DBS DC target	[codes]	-2^{15}	$+2^{15}-1$	-2^{15}	$+2^{15}-1$
Trigger level	[codes]	-2^{15}	$+2^{15}-1$	-2^{15}	$+2^{15}-1$
Reset level	[codes]	-2^{15}	$+2^{15}-1$	-2^{15}	$+2^{15}-1$
Trigger arm hysteresis	[codes]	0	$+2^{15}-1$	0	$+2^{15}-1$
Reset arm hysteresis	[codes]	0	$+2^{15}-1$	0	$+2^{15}-1$
Raw data detection					
Pulse width (TOT)	[samples]	1	-	1	-
Pulse separation	[samples]	1	-	1	-
Record length	[samples]	16	$2^{32}-1$	32	$2^{32}-1$
Leading edge window (LEW)	[samples]	0	2^{14}	0	2^{14}
LEW granularity	[samples]	16	-	32	-
Trailing edge window (TEW)	[samples]	0	2^{30}	0	2^{30}
TEW granularity	[samples]	16	-	32	-
Pulse characterization detection					
Pulse height	[codes]	-2^{15}	$+2^{15}-1$	-2^{15}	$+2^{15}-1$
Computed pulse width[3]	[samples]	1	$2^{16}-1$	1	$2^{16}-1$
Pulse separation	[samples]	1	-	1	-
Pulse peak time stamp[4]	[samples]	-	$2^{32}-1$	-	$2^{32}-1$
Average pulse rate per channel[5]	[10^6 pulses/s]	-	300	-	600
Pulses per burst at highest intensity per channel[6]	[10^6 pulses/s]	-	1250	-	2500
Pulses per detection window per channel	[samples]	0	$2^{29}-1$	0	$2^{30}-1$

1. The 14-bit data word is mapped MSB-aligned to a 16-bit signed integer.
2. See the 16-1796 ADQ7DC manual for details on DC-offset.
3. The number of samples between the pulse trigger and the reset level.
4. The number of samples between the detection window trigger and the peak value.
5. Assuming PCIe data transfer rate at 5 Gbytes/s to PC. The pulse rate is reduced if the data transfer rate is lower than 5 Gbytes/s.
6. The highest pulse rate is one pulse every second sample. This is the maximum allowed number of pulses at that rate. Above that, the average pulse rate applies.

Table 2: Definitions and acronyms, Figure 2.

	DEFINITION	COMMENT
Acronyms		
DBS	Digital baseline stabilizer	Teledyne SP Devices' proprietary IP.
LEW	Leading edge window	Samples before trigger (pre-trigger).
TEW	Trailing edge window	Samples after end of pulse.
ADC	Analog-to-digital converter	
API	Application programming interface	
FWPD	Pulse detection firmware for Teledyne SP Devices digitizers.	
GUI	Graphical user interface	
MSPS	10^6 samples per second	
GSPS	10^9 samples per second	
GBPS	10^9 bytes per second	
TOT	Time-over-threshold	Same as pulse width, see below.
SDK	Software development kit	
Definitions		
Header	Information about the record.	
Peak	Extreme value of a pulse.	Maximum value if triggering on rising edges. Minimum value if triggering on falling edges.
Pulse	The samples between a trigger event and a reset event.	
Record	A set of data belonging to a trigger.	The data set can be consecutive samples (raw data), analysis data, or padding.
Reset event	An event that defines the end of a pulse.	The last reset event defines the end of a record.
Time stamp	A value that gives a real-time timing of a record.	
Trigger event	An event that defines the start of a pulse or a detection window.	The first trigger event starts the acquisition of a record.
Pulse width	The time between a trigger event and a reset event of a pulse.	This is also called time-over-threshold (TOT).

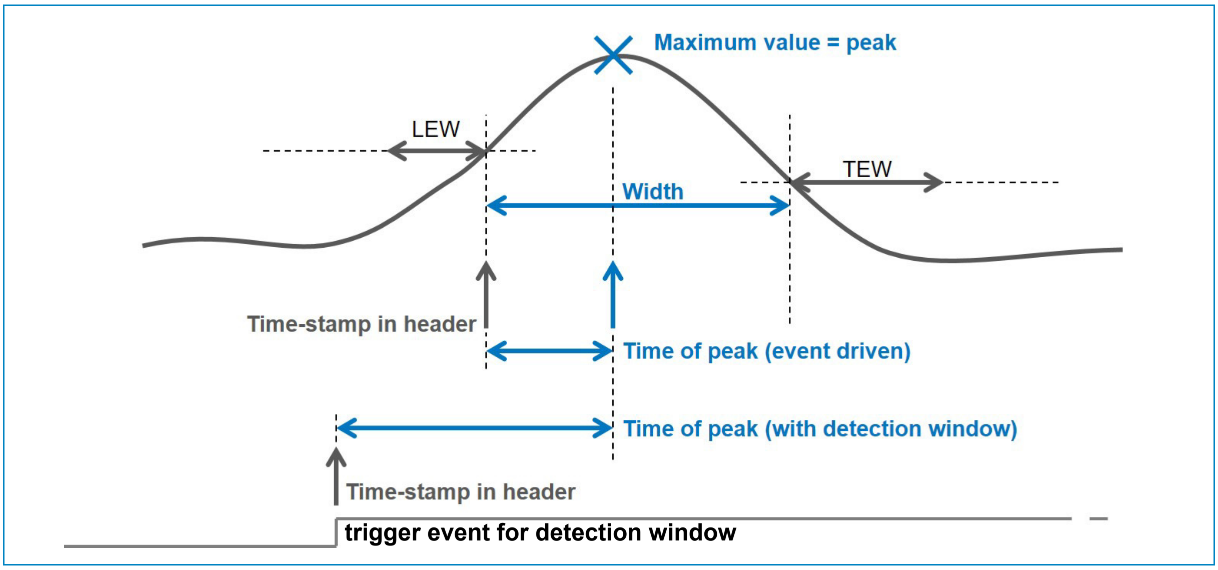


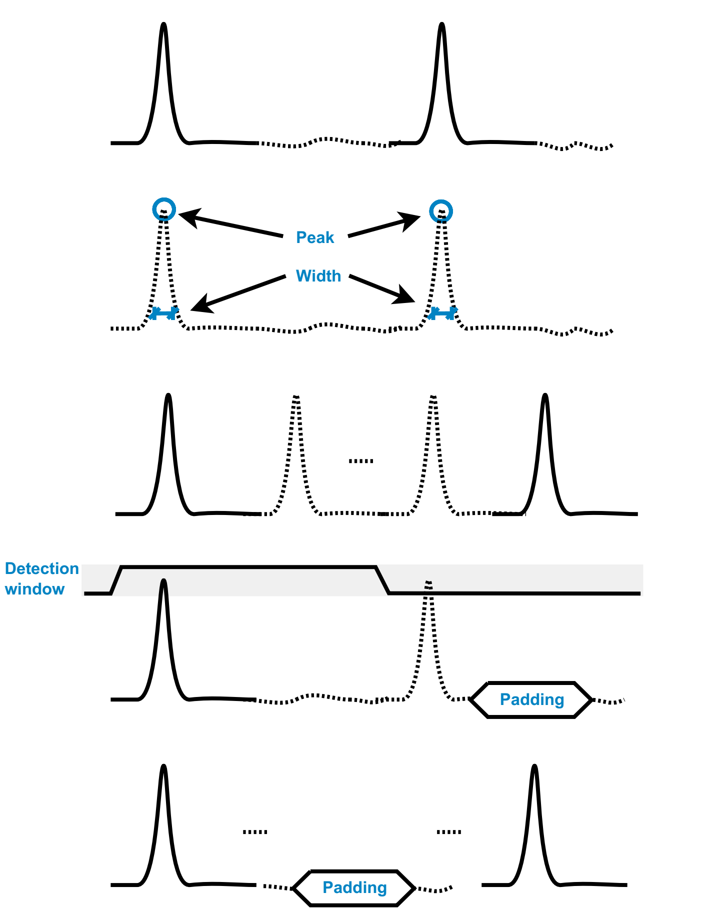
Figure 2: Pulse definition in standard implementation of –FWPD.

Trigger and collection modes supported by –FWPD

Table 3 shows all valid combinations of operational modes and triggers. Note that all modes support multi-unit synchronization for multi-channel systems. Figure 3 illustrates and describes the five available data collection modes. The padding feature in the mode 3 and mode 4 are intended for applications where the pulses are sparse. Padding with records of dummy data (zeros) allows for a guaranteed minimum throughput.

Table 3: Trigger modes

MODE	TRIGGER		SYNC OF CHANNELS		RECORD LENGTH		PADDING
	DATA	DETECTION WINDOW	INDIVIDUAL	SIMULTANEOUS	VARIABLE	FIXED	
0	Level		✓		✓	✓	
	SW / EXT / INT			✓		✓	
2	Level		✓		✓	✓	
	SW / EXT / INT			✓		✓	✓
3	Level	SW / EXT / INT			✓	✓	✓
4	Level		✓		✓	✓	✓
	SW / EXT / INT			✓		✓	✓



Mode 0. Raw pulse data (default).

Mode 0, 2 and 3. Pulse analysis data is collected and sent on a separate data channel.

Mode 2. Every *N*th pulse is collected.

Mode 3. Raw pulse data with padding, detection window enabled. A padding record is added to ensure an minimum latency of the system, independently of how frequent the pulses are.

Mode 4. Raw pulse data with padding, detection window disabled.

Figure 3: Data collection modes of –FWPD. Solid pulse lines illustrate collected data. Dotted pulse lines correspond to suppressed data.

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Worldwide Sales and Technical Support

www.spdevices.com

Teledyne SP Devices Corporate Headquarters

Teknikringen 6
SE-583 30 Linköping
Sweden

Phone: +46 (0)13 465 0600
Fax: +46 (0)13 991 3044
Email: info@spdevices.com