ADQ3-FWPD Datasheet

The ADQ3-FWPD is a real-time pulse detection and pulse analysis FPGA firmware for the high-end ADQ3-series digitizers. ADQ3-FWPD adds pulse attribute calculations to the standard firmware FWDAQ.

Ordering information

- Firmware option FWPD for ADQ3-series of digitizer, order code **ADQ3-FWPD**.
- FWPD combined with firmware development kit, **ADQ3-DEVPD** (available 2024)

Compatible hardware models

- ADQ30 single-channel mode
- ADQ32 single- and dual-channel modes
- ADQ32-PDRX combined channels and dual-channel mode (not combined)
- ADQ33 dual-channel mode
- ADQ33-PDRX combined channels and dual-channel mode (not combined)
- ADQ35 single- and dual-channel mode
- ADQ35-WB single- and dual-channel mode
- ADQ35-PDRX combined channels and dual-channel mode (not combined)
- ADQ36 in dual- and quad-channels modes

1 ADQ3-FWPD INTRODUCTION

1.1 Features

- Compliant with features of FWDAQ
  - Frame pulses using trigger blocking
  - Detect pulses using level trigger
  - Correct baseline using Digital baseline Stabilizer (DBS)
  - Timestamp for pulse time determination
  - Daisy-chain trigger distribution concept for large arrays of detectors
- Data rate reduction in the FPGA of the digitizer by computing attributes of pulses
- Data and attributes transferred as separate channels for flexible selection of operating mode
- Pulse attribute calculations:
  - Area (sum)
  - Full width half max (FWHM)
  - Time of pulse peak
  - Maximum pulse amplitude
  - Centroid of peak
  - Open FPGA allows for customization of attributes

1.2 Applications

- Time-of-flight mass spectrometry
- LiDAR
- Neutron time-of-flight
- High energy physics
- Other types of pulse detection

1.3 Advantages

- Efficient implementation of pulse detection and analysis in the FPGA off-loading the PC
- Optimized for real-time processing and high data throughput
- Teledyne SP Devices' design services are available for fast integration to reduce time-to-market

2 BLOCK DIAGRAM

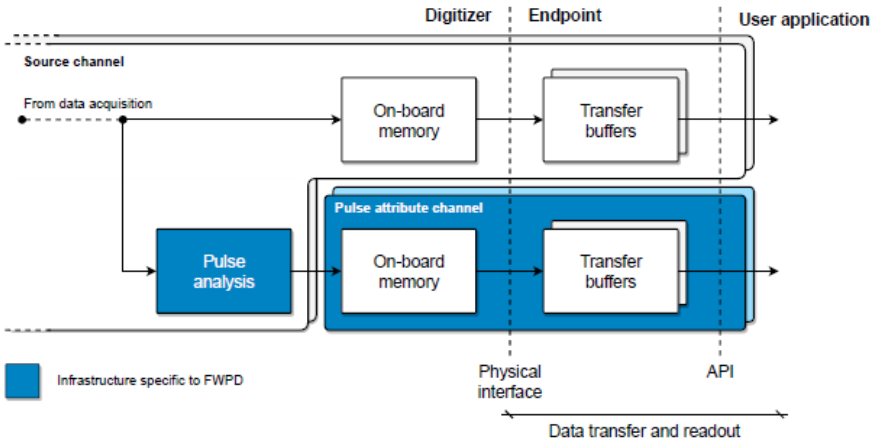

Figure 1 Block diagram of FWPD. FWPD adds attributes computations and attributes channels to the functions in standard firmware FWDAQ.

3 PULSE DETECTION AND ANALYSIS – PRINCIPLE OF OPERATION[1]

3.1 DBS – Digital Baseline Stabilizer

The DBS analyses the signal and subtracts the DC-offset. This creates a stable reference point for computing pulse-related parameters. The DBS actively compensates for slow baseline shifts such as temperature variations, supply voltage drift and aging, and stabilizes the baseline to a level corresponding to 22-bit precision. The DBS also compensates for pattern noise in interleaved ADCs.

3.2 General-purpose FIR filter

The general-purpose FIR filter enables the suppression of noise in a certain frequency band. The FIR filter is user-controlled so that it can be optimized for the specific application/system.

3.3 Detection window

The detection window defines where to search for pulses. It is controlled by an event (trigger) and a length parameter. The detection window is comparable to the term “record” in the standard acquisition mode.

3.4 Pulse detection

Pulse detection is handled by level triggering. The start of a pulse occurs when the signal level is passing a level and end of a pulse occurs when the signal is passing the same level from the opposite direction. The direction is depending on the polarity of the pulse.[2] A leading-edge window and a trailing-edge window define additional samples that belong to the pulse.

3.5 Multi-peak for close pulses

Pulses close to each other may not activate the level trigger level. There is an additional multi-peak detection mechanism that uses a dynamic threshold to identify these pulses.

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[1] All features in this section except for the computation of attributes and the attributes data channel and multi-peak are available in standard firmware FWDAQ.

[2] The polarity of the pulses is set by the user. The FWPD can only handle one polarity per channel.

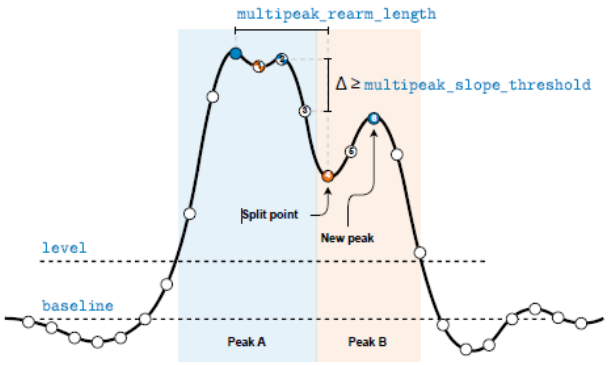

Figure 2 Illustration of multi-peak from user guide 21-2539.

3.6 Pulse attributes analysis

A set of standard attributes is calculated for each pulse in FWPD. The attributes can be replaced by custom attributes using the open FPGA.[3] The standard attributes are

- Time of pulse peak
- Area (sum) of pulse
- Full width at half maximum (FWHM)
- Peak amplitude
- Centroid

The 21-2539 user guide of ADQ3 digitizers contains a detailed definition of how the attributes are computed.

The attributes are sent to the host PC on a separate attributes channel. The digital output of the board thus has twice as many channels as analog input channels.

[3] Custom attributes computations can be implemented using the open FPGA. The open FPGA is accessed through the development kit with order code DEVDAQ. Note that multi-peak is not available in DEVDAQ. For customization of attributes including multi-peak, contact Teledyne SP Devices for more information.

4 SYSTEM DESIGN USING FWPD

4.1 System design optimization and streaming to PC

FWPD is used in measurement systems where detectors and the digitizer operate in a real-time. The purpose is to reduce the computational load on the PC.

The FWPD firmware implements the most demanding core processing inside the FPGA. Attributes channel is expected to have a reduced data rate compared to the raw data channel. By turning off the raw data and activating only attributes, the data rate is reduced.

The streaming of data to the PC is done in parallel with the recording without introducing any dead-time.

See the ADQ3-series user guide for instructions on how to tune parameters for optimal performance.[4]

4.2 Large arrays of detectors

Use the Daisy-chain trigger distribution for synchronization of large arrays.

4.3 Scheduling for high performance and data safety

FWPD is designed to operate constantly over a long time with data-driven operation. The momentary pulse density sets the data rate and there are multiple features to support the necessary data transfer and processing:

1. There is an onboard FIFO to manage data rate variations as well as unexpected interrupts in the PCIe data transport.
2. There is a controlled data discard in case of an overflow due to interrupts anywhere in the processing chain.
3. There is an auto-recover and resynchronization feature in case of lost data. This is useful for very long measurement operations. In case of an unexpected interrupt in the data transport which cannot be handled by the FIFO, the FWPD firmware maintains the grid established by the trigger source. It is not necessary to restart the system to continue the measurement.
4. The data readout is thread-safe and multiple threads can operate on the data. This increases the processing capacity of the system.

[4] ADQ3-series user guide with document number 21-2539 can be downloaded from www.spdevices.com

5 TECHNICAL DATA

See 21-2539 ADQ3 series digitizers user guide revision 2026.1 or later for limitations on pulse density and parameter settings.

Table 1 Attributes

Attribute	Description	Size [bytes]
Time	Time of peak value	4
Area	Area (sum) of pulse	4
FWHM	Full width half max	2
Peak value	Value of largest sample	2
Centroid	Centroid position	3
Status	Information about attributes	1

Table 2 Software support

Parameter	Value
Operating system[5]	Windows / Linux
GUI	Digitizer Studio
Example code	C, Python
API	C / C++

[5] See 15-1494 Operating system support for a detailed listing of supported distributions.

Table 3 Data transfer rate

Mode	Description	Data set per trigger[6]
Continuous recording[7] of original signal	Continuous recording of raw data from original signal	PCIe transfer rate limits the recording
Detection window /record[7]	All data within a detection window is recorded as one record	Record length + header[8]
Pulse detection / zero suppression[7]	Samples which belong to pulses are recorded	Average number of pulses * (header[8] + average pulse length)
Pulse attributes[9]	Computed attributes of pulses	Header[8] + 16 bytes * average number of pulses[10]

[6] Average data rate is triggering rate multiplied with size of data set.

[7] Available in FWDAQ and FWPD.

[8] The header is 72 bytes.

[9] Requires FWPD. Not available in FWDAQ.

[10] Each pulse result in 16 bytes of attribute data

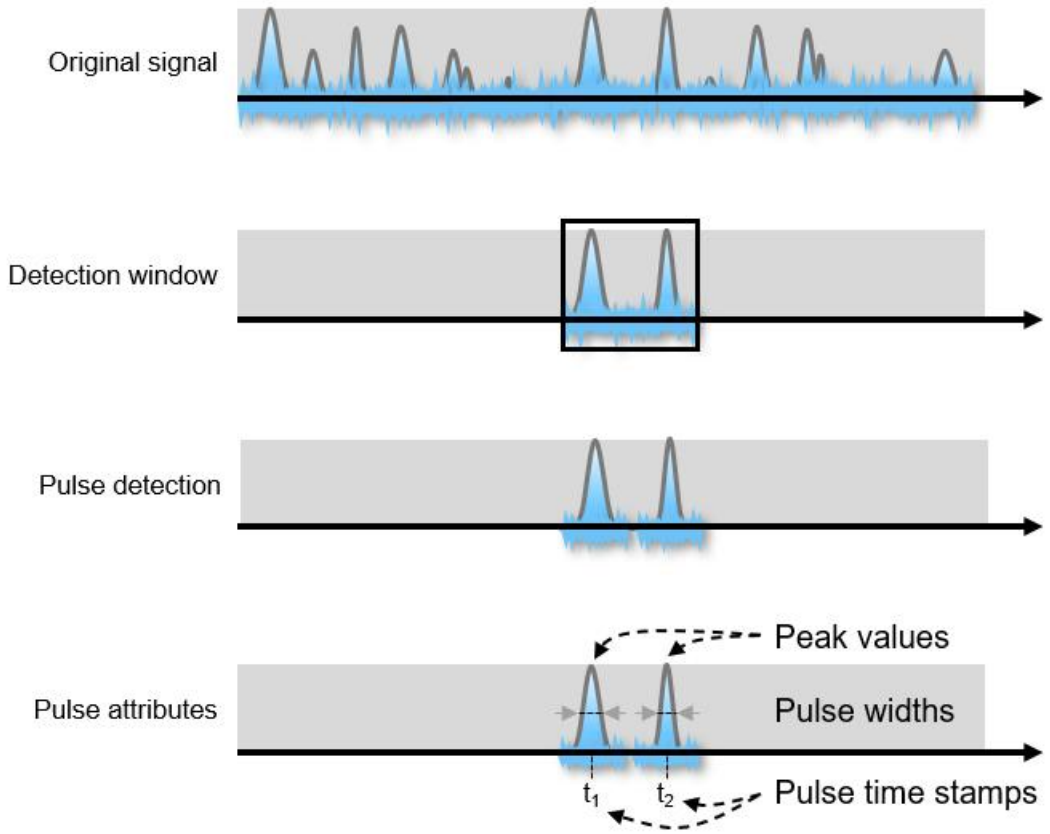

Figure 3 Pulse detection and analysis, principle of operation

6 CHANGING NUMBER OF CHANNELS

Some hardware models support both one and two channels operation. Changing from two channels to one channel is done by changing firmware image in the FPGA. Both firmware images are stored in the non-volatile memory of the digitizer. Use the software tool ADQAssist to change boot image. Changing firmware requires power cycling of the PC for the PCIe bus to enumerate.

7 BLOCK DIAGRAM

Below are block diagrams for FWPD installed in various hardware configurations.

The User Logic 1 and User Logic 2 blocks are available for the user through the Firmware Development Kit, DEVPD, which is ordered separately and available in 2024.

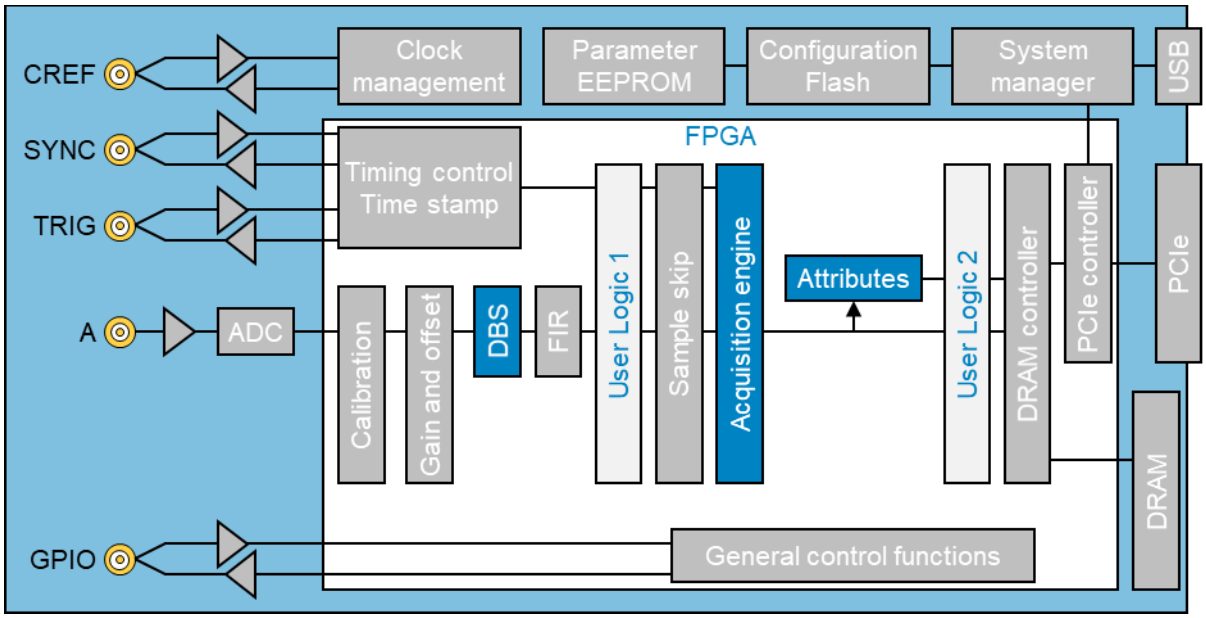

Figure 4 Block diagram for FWPD installed on a single-channel digitizer.

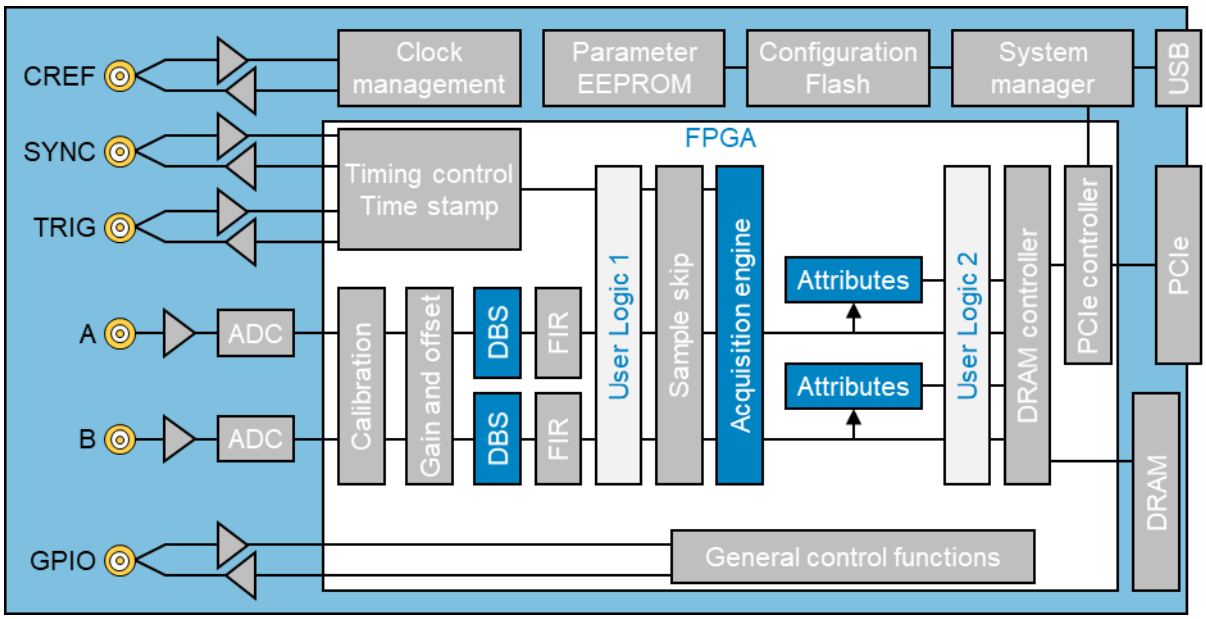

Figure 5 Block diagram for FWPD installed on a dual-channel digitizer.

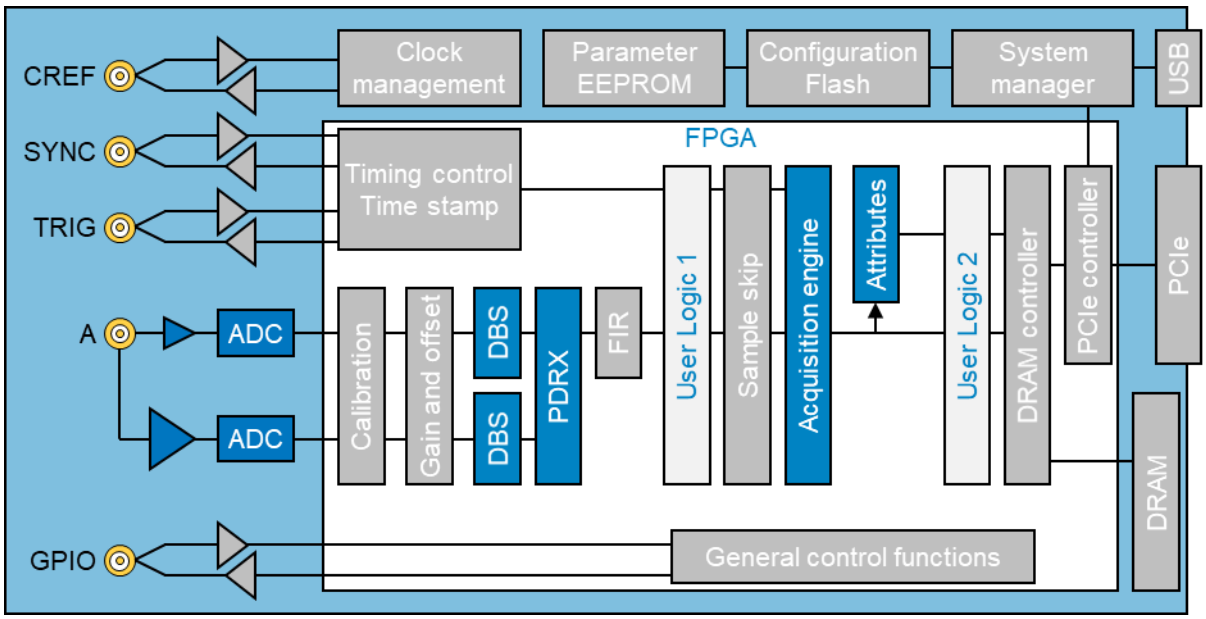

Figure 6 FWPD combined with PDRX, illustrated with channel combination activated.

Figure 7 Typical digitizer in the ADQ3 family.

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