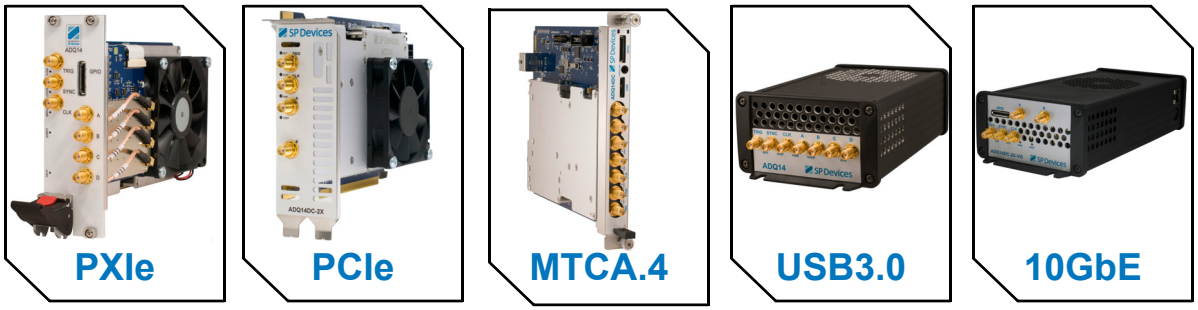
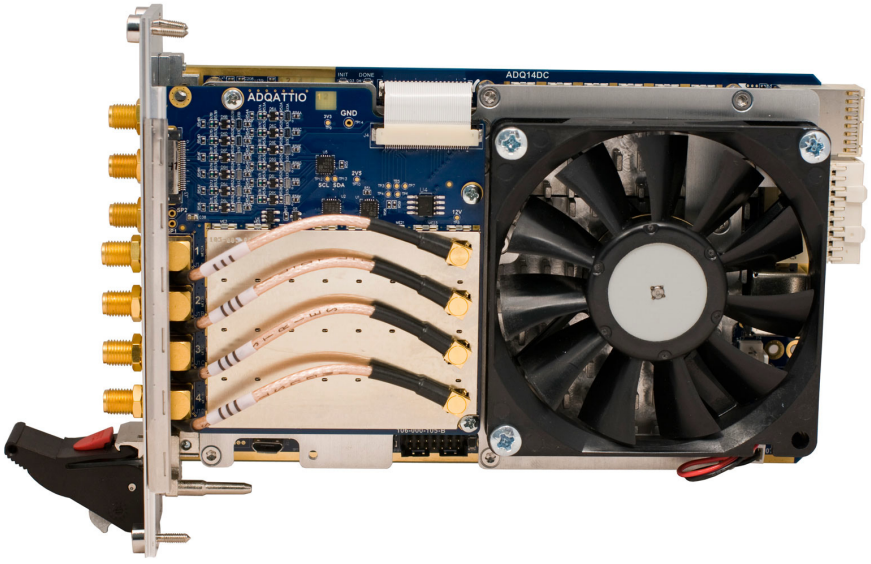
ADQ14-FWSDR firmware datasheet



ADQ14-FWSDR Software Defined Radio firmware with these features:

- *Digital Down Conversion*
- *Decimation filtering*
- *Streaming data.*



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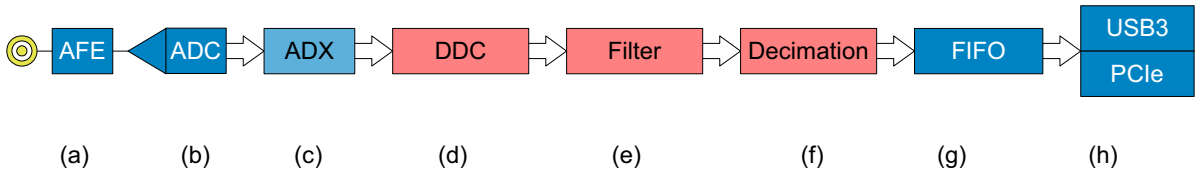
1 Principle of operation

The purpose of the ADQ14-FWSDR firmware option is to implement efficient radio receiver for general purpose radio architecture.

On interleaved models of ADQ14, the ADQ14-FWSDR benefit from the powerful ADX interleaving technology from SP Devices. ADX enables interleaving of ADCs to get wide bandwidth.

The principle structure of the ADQ14-FWSDR is shown in **Figure 1**.



#	DESCRIPTION	USER CONTROL	REF
a	The analog front-end is either DC- or AC-coupled.	See ADQ14 Manual	3.2
b	The high performance 14-bit A/D Converters are interleaved on –2X and –1X models to reach higher bandwidth.		3.2
c	SP Devices provides proprietary IP for signal enhancement, The ADX is an algorithm for interleaving of A/D converters which his is available on interleaved models.	ADX control commands	3.3
d	The quadrature mixer transforms the center frequency to the pass-band of the decimation filters.	*SetMixerFrequency* *SetMixerPhase* *SetTimestampSync*	3.4
e	The decimation reduces the sample frequency.	*SetSampleDecimation*	3.5
f	The filter reduces the bandwidth and the noise level. The filter can also implement an equalizer or IQ balance.	*SetEqualizerSDR*	3.6
g	The FIFO handles the conversion from the real-time radio and the interrupt controlled PC.	*SetDataFormat*	3.7
h	Connection to the host PC	See ADQ14 Manual	3.7

Figure 1: Principle of the ADQ14-FWSDR.

2 Configuration options

There are several ways of configuring the ADQ14-FWSDR for a radio application. Below are some examples.

2.1 I and Q IF receiver

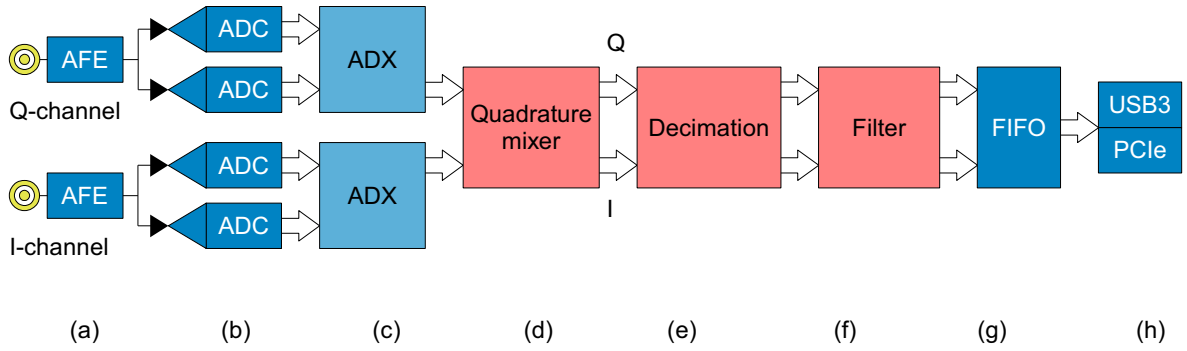


Figure 2: ADQ14-FWSDR configured as wide-band I and Q receiver.

2.2 Dual channel I and Q IF receiver

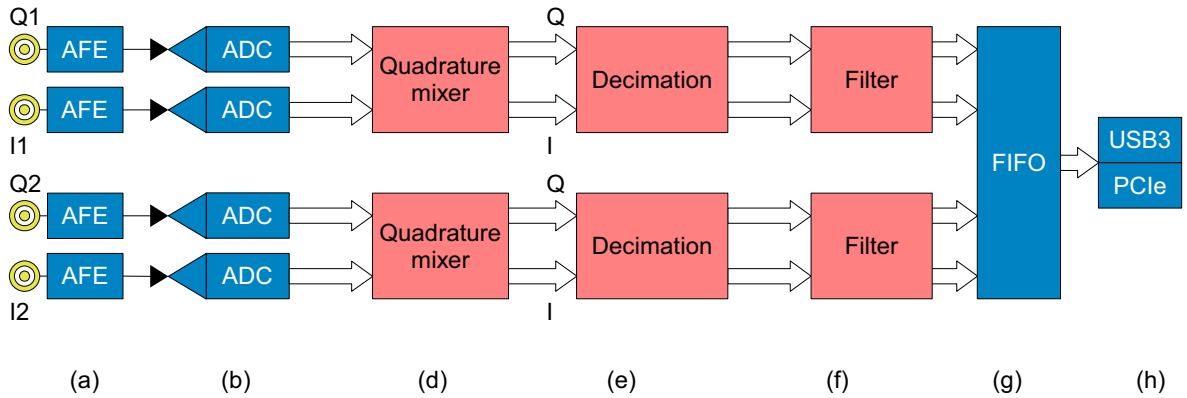


Figure 3: ADQ14-FWSDR configured as two I and Q channels.

2.3 Differential inputs

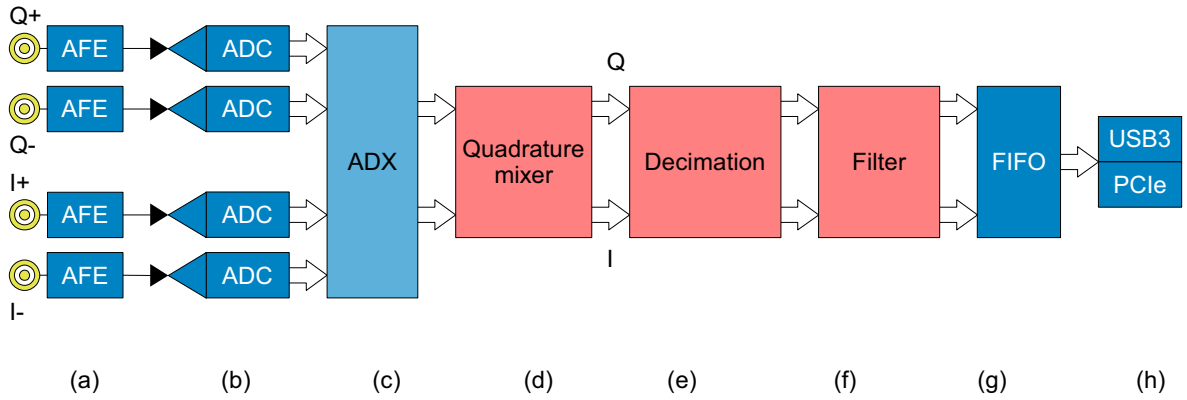


Figure 4: ADQ14-FWSDR configured for differential inputs.

3 Block description

3.1 Configurations

The configuration with interleaved 2 GSPS inputs is shown in **Figure 5** and non-interleaved 1 GSPS is in **Figure 6**. The ADQ14-4C in **Figure 6** does not contain HB1, since the data rate from the ADC is only 1 GSPS.

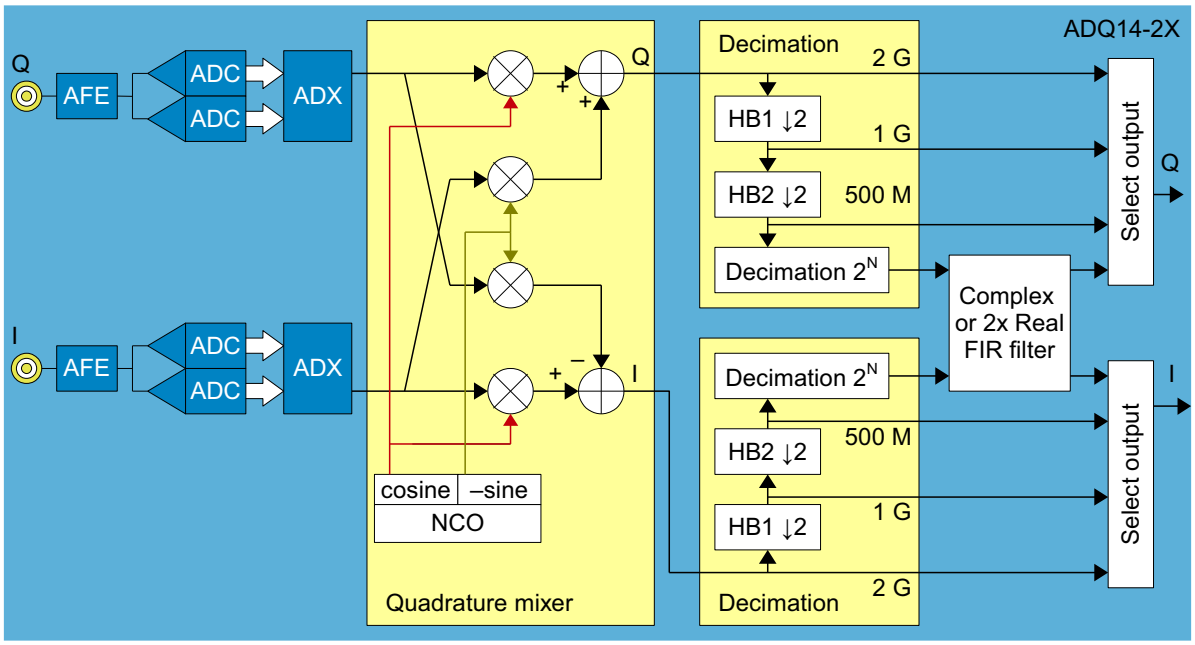


Figure 5: ADQ14-FWSDR DDC and filter details for interleaved inputs.

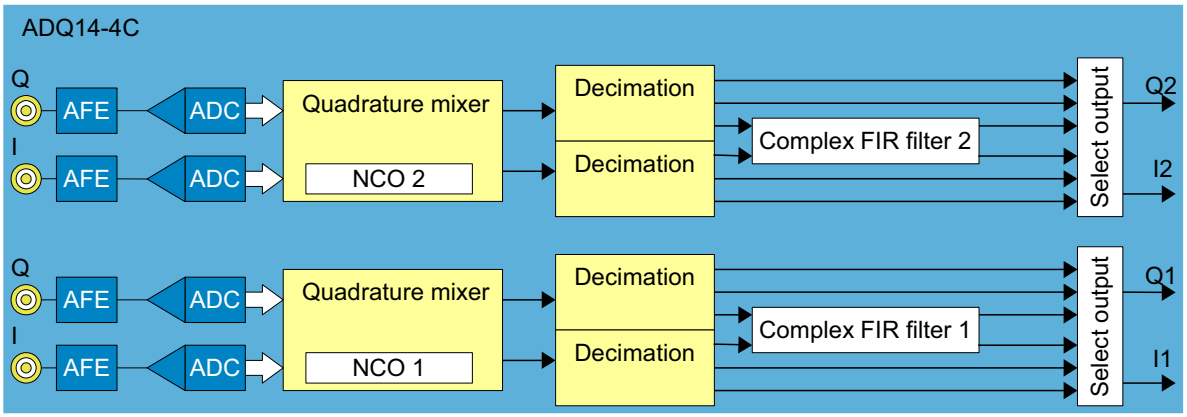


Figure 6: ADQ14-FWSDR DDC and filter details for 4 inputs.

3.2 Analog input

The analog front-end is AC-coupled on ADQ14AC. This is preferred for high IF applications, since the AC-coupled front-end is the best choice for linearity at high frequencies.

The DC-coupled front-end is intended for low (or zero) IF systems. It is also preferred where a high sensitivity is beneficial since the full scale signal range is as low as 500 mVpp on ADQ14DC-4C. This reduce the need for additional amplifiers before the ADQ14.

The DC-coupled front-end is also available with a variable gain option, –VG, for a full flexible test and measurement solution.

3.3 ADX

ADX is placed right after the A/D conversion. ADX is a proprietary technology from SP Devices, which improves the signal quality for a wide bandwidth.

ADX operates in the background and is automatically updating parameters using all available incoming signals.

#	DESCRIPTION	PARAMETER	
	Typical time-interleaving spur level	–75 dBc	

Table 1: ADX parameters.

3.4 Quadrature mixer

The quadrature mixer converts the signal frequency from the incoming signal band to the pass-band of the decimation filters. The Numerically Controlled Oscillator (NCO) operates as Local Oscillator (LO).

It is possible to use different frequencies on different digitizer channels in order to receive different frequency bands. It is also possible to control the phase of each NCO individually for phased array applications. Use the commands ***SetMixerFrequency*** and ***SetMixerPhase*** to control the quadrature mixer. The NCOs of several cards are synchronized by the method ***SetTimestampSync***.

#	DESCRIPTION	PARAMETER	
	NCO frequency resolution	0.1 Hz	
	NCO SFDR	95 dB	

Table 2: DDC and NCO parameters.

3.5 Decimation

The low-pass filter reduce the signal bandwidth and the decimation reduce the sample rate. For a radio receiver system, the order of decimation is generally low. The goal is to reduce the data rate as much as possible to be able to stream data to the host PC.

The first filters, HB1 and HB3 are half-band FIR filters with fixed coefficient. In each of these stages, the data rate is reduced by a factor of 2.

The last stage is a high order (up to 2^31) decimation function. This is used for scanning with very high precision to measure, for example phase noise measurements.

High order of decimation increases the SNR. It can therefore be beneficial to change from 16 bits to 32 bits representation. The data word size is set by the software command ***SetDataFormat***.

The decimation factor is the same for all channels, and it is set by the command ***SetSampleDecimation***.

#	PARAMETER	HB1	HB2	HIGHER ORDER DECIMATION
	Pass band ripple	0.01 dB	0.01 dB	0.01 dB
	Stop band attenuation	–125 dB	–125 dB	–105 dB
	Bandwidth	35 %	35 %	40 %
	Decimation factors	2	2	1 to 2^31

Table 3: Filter parameters.

3.6 Filter, Equalizer or IQ balance

The filter is a general-purpose complex FIR-filter with user-controlled coefficients. The filter may also be configures as two individual real valued filter. This filter is general purpose, but the position in the signal

chain makes it suitable for an equalizer function. By configuring the filter as a complex FIR, it can be used for IQ-balancing.

The filter is configured with the command ***SetEqualizerSDR***.

#	PARAMETER	VALUE	
	Filter length, maximum number of coefficients	15	
	Maximum filter coefficient	$2 - 2^{-14}$	
	Minimum filter coefficient	–2	
	Filter coefficient word length	16 bits	
	Input data word length maximum	25 bits	

Table 4: Equalizer filter parameters.

3.7 FIFO.

Data rate from the SDR firmware is real-time. To handle the non-real-time behavior in the host PC, there is a 2 GByte data FIFO on the ADQ14.

3.8 PC host interface

The interface to the host PC is USB3.0 or PCIe, depending on the selected hardware model. The ADQ14-FWSDR supports record acquisition and continuous streaming to the host PC.

4 Acquisition modes.

4.1 Continuous streaming mode

Continuous streaming means that there is a continuous flow of data from the start until the end of the measurement. This is one single long recording. At the beginning of the recording is a header telling when the acquisition started (see 15-1593 ADQ14 Manual for information about record header and time-stamp).

To use continuous streaming, the data rate has to be reduced by decimation. The maximum capacity is determined by the ADQ14 in combination with the host PC and possibly also the disk write speed. ADQ14 is capable of streaming up to 3.2 GBytes/s to the PC RAM.

Example: The minimum data rate required by the application is double the signal bandwidth. (In practice, a little margin is required for filters.) For example, a 50 MHz signal requires 100 MSPS minimum. The pass-band of the decimation filter is 40%, so in practice 50/0.4 = 125 MSPS is a good choice. For an I and Q zero-IF representation, this means 62.5 MSPS on I and Q branch.

- In a ADQ14-2X (2 GSPS), set the decimation factor to 32 to get 2000/32 = 62.5 MSPS, **Figure 5**.
- In a ADQ14-4C (1 GSPS), set the decimation factor to 16 to get 1000/16 = 62.5 MSPS, **Figure 6**.

Each sample is 2 bytes. Thus I and Q together will result in 62.5 MSPS X 2 bytes/sample X 2 = 250 MBytes per second data rate to the PC.

4.2 Triggered streaming mode

Triggered streaming means that associated to each trigger event is a known and limited recording time.

Each record contains a header with time-stamp of the trigger time.

The average data rate is then *Record Length X Trigger Rate*. Thus data rate to the PC is controlled by these parameters.

For burst recording, the DRAM on the card can be used. The system is then independent of the data rate to the PC. The total amount of data *Record Length X Number of Records* has to fit into the memory of 2 GBytes.

5 Using ADQ14-FWSDR

5.1 Connecting to a host PC for data storage

Use the ADQ14-FWSDR signal processing capability to adjust the data rate. The data rate has to match the signal bandwidth according to the sampling theorem. The data rate in the transfer to the PC is limited to 3.2 GBytes/s. The ADQAPI supports data transfer to user's buffers in the API. From those buffers, the application software[1] can use the data or store it on a disk.

1. Application software is designed and implemented by the user.

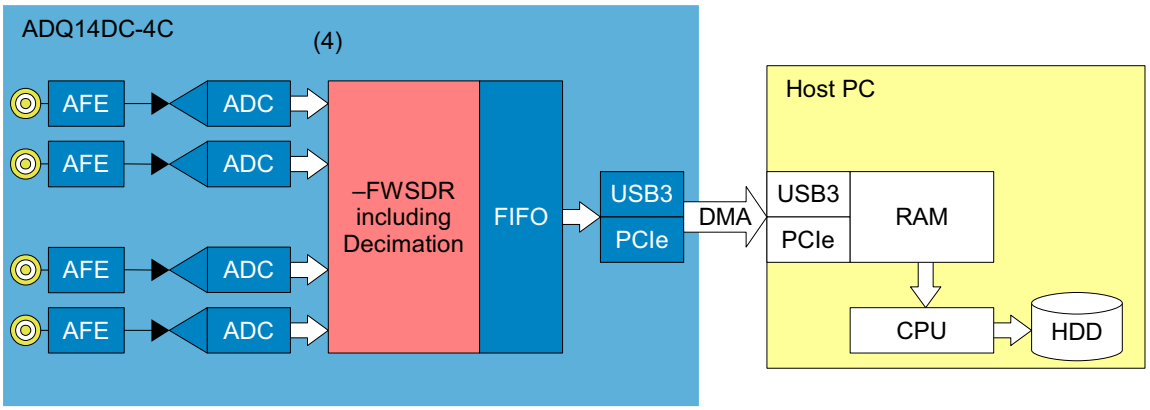
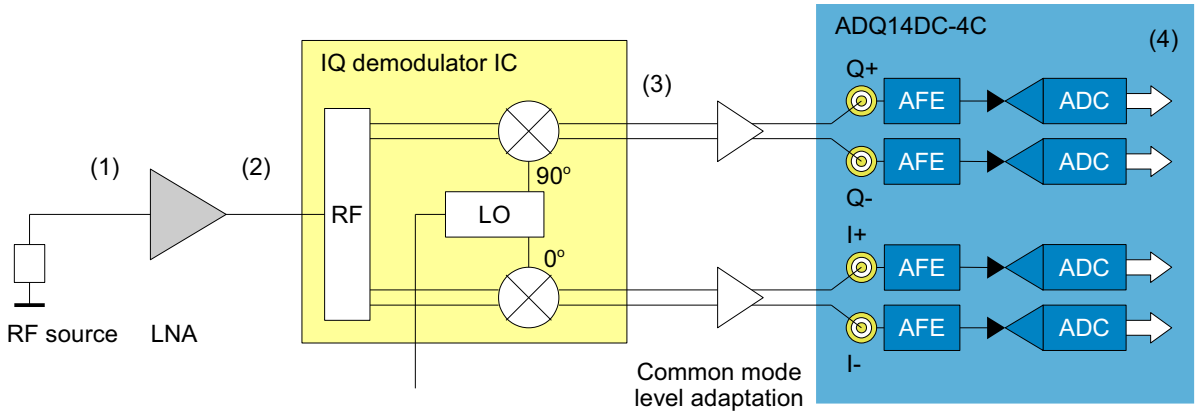


Figure 7: ADQ14-FWSDR storing data to disk.

5.2 DC-coupled AFE with Zero-IF IQ demodulator IC.

Figure 8 and Table 5 shows ADQ14DC in an example system with a typical IQ-demodulator.



#	DESCRIPTION	USER CONTROL	REF
a	The source is modeled with a 50 Ohm resistor.		
b	The LNA.		
c	A IQ demodulator typical single chip IC. The output is DC-coupled with differential signaling. The output is Zero-IF In-phase and Quadrature.		
d	Match the common mode level of the IQ demodulator output and the ADQ14 inputs.		

Figure 8: Connecting to a differential Zero-IF IQ Demodulator.

6 Synchronization

6.1 Phase lock NCOs

The NCOs can be phase locked to the external (or internal) 10 MHz clock reference. This is done by setting up the system similar to **Figure 9**.

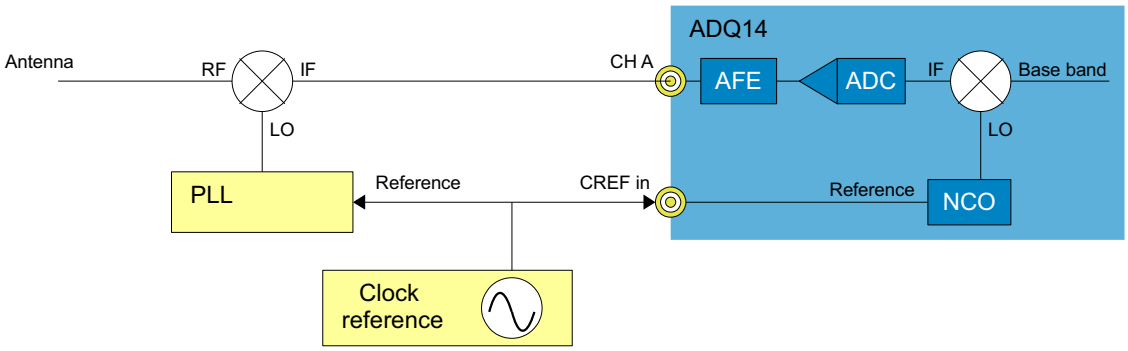


Figure 9: ADQ14-FWSDR principle of clock reference distribution

The NCOs in the ADQ14 can be locked to the clock reference as in **Figure 10**. Set up the digitizer to wait for an external SYNC signal[1]. The NCOs are phase locket to 10 MHz reference at the clock edge following after the sync signal. Time-stamp is also reset with this signal.

The phase and frequency of each NCO is set individually, which is useful for phased array applications.

1. The external trigger may also be used. This is set by a software command.

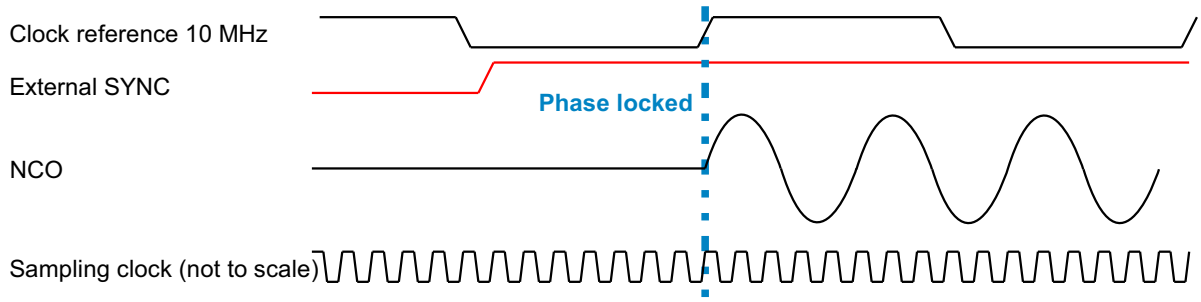


Figure 10: ADQ14-FWSDR phase lock to external 10 MHz reference

6.2 Synchronizing several ADQ14-FWSDR

By distributing the SYNC signal and the clock reference to several ADQ14-FWSDR, fully synchronous multi-channel system is achieved.

6.3 Synchronized acquisition.

Both acquisition modes, **Section 4**, are started with a trigger event. When using the phase lock function of **Section 6.1**, all triggers are blocked until the synchronization is completed. Then the acquisition will start on the first trigger.

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