ADQ36-PXIe Datasheet

The ADQ36-PXIe is a high-end 12-bit quad channel flexible data acquisition board optimized for use in high channel-count scientific applications. The ADQ36 features:

- **4 / 2 analog input channels**
- **2.5 / 5 GSPS per channel**
- **7 GBytes/s sustained data transfer rate**
- **Two external triggers**
- **General Purpose Input/Output (GPIO)**

Ordering information

- ADQ36-PXIe digitizer including firmware FWDAQ, order code **ADQ36-PXIe**.
- Warranty extension to 5 years for ADQ36, order code **ADQ36 -W5Y**.[1] [2]
- Firmware development kit for FWDAQ, order code **ADQ36-DEVDAQ**.

[1] Included warranty is 3 years from the date the product is shipped by Teledyne SP Devices. The option extends the warranty to 5 years from the date the product is shipped by Teledyne SP Devices.

[2] Warranty extension must be ordered before included 3 years warranty is expired.

1 ADQ36 INTRODUCTION

1.1 Features

- 4 / 2 analog input channels, software-selectable
- 2.5 / 5 GSPS sampling rate per channel
- 12 bits vertical resolution
- DC-coupled with 2.5 GHz analog bandwidth
- Programmable DC-offset
- Internal and external clock reference
- Internal and external clock source
- Clock reference output
- Internal and external triggers
- 8 GBytes data memory
- 7 GBytes/s sustained data streaming to CPU and GPU
- Data interface PXIe Gen3 x8

1.2 Applications

ADQ36 is intended to be used primarily in high channel-count systems.

- LIDAR
- Beam Position Monitor
- High energy physics

1.3 Advantages

- A compact high-performance digitizer that optimize the system solution
- Real-time processing and high data throughput
- Teledyne SP Devices' design services are available for fast integration to reduce time-to-market

1.4 System design optimization; open FPGA and streaming to CPU and GPU

High-performance data acquisition systems require high-speed real-time analysis. ADQ36 offers a variety of options for efficient system design:

Streaming to GPU
ADQ36 supports up to 7 GByte/s peer-to-peer streaming and streaming via pinned buffer to GPU. A GPU offers a powerful platform for implementing application-specific signal processing algorithms.

Streaming to CPU
ADQ36 supports up to 7 GByte/s to host PC. Implementing the application-specific algorithms in the CPU results in an efficient system.

Open FPGA for real-time processing
ADQ36 offers an open FPGA for implementation of the application-specific computations in the FPGA. This gives the most compact system design.

2 TECHNICAL DATA

Technical parameters are valid for ADQ36 operating with firmware FWDAQ. All parameters are typical unless otherwise noted.

Table 1 Analog input (front panel label A, B, C and D)

Parameter	Condition	Unit	Min	Typical	Max
Basic parameters					
Number of channels[3]	4-channel mode			4	
Sampling rate per channel	4-channel mode	Gsample/s		2.5	
Number of channels	2-channel mode			2	
Sampling rate	2-channel mode	Gsample/s		5	
Bandwidth (-3dB)		GHz		2.5	
Input range		Vpp		0.5	
Input impedance		Ω		50	
Coupling				DC	
Programmable DC-offset					
DC-offset range		V	-0.25		+0.25
AC performance, 4-channel mode, 2.5 GSPS					
Cross talk	< 800 MHz	dBFS		-70	
Noise power density	0 to 1.25 GHz	dBFS/√Hz		-148	
SNR	260 MHz, -1dBFS	dBc		54	
SFDR	260 MHz, -1dBFS	dBc		65	
ENOB relative full scale	10 MHz, -1dBFS	bits		8.8	
ENOB relative full scale	260 MHz, -1dBFS	bits		8.8	
ENOB relative full scale	810 MHz, -1dBFS	bits		8.8	
ENOB relative full scale, using FIR filter[4]	260 MHz, -1dBFS	bits		9.0	
AC performance, 2-channel mode, 5 GSPS					
Cross talk	< 800 MHz	dBFS		-80	
Noise power density	0 to 2.5 GHz	dBFS/√Hz		-150	
SNR	260 MHz, -1dBFS	dBc		53	
SFDR	260 MHz, -1dBFS	dBc		60	
ENOB relative full scale	10 MHz, -1dBFS	bits		8.7	
ENOB relative full scale	260 MHz, -1dBFS	bits		8.6	
ENOB relative full scale	1625MHz,-1dBFS	bits		8.1	
ENOB relative full scale, using FIR filter[4]	260 MHz, -1dBFS	bits		9.0	

[3] The number of channels is configured by changing firmware of the FPGA. Changing firmware requires a re-boot of the PC. Both 4-channel and 2-channel modes are included in the delivery.

[4] Programmable FIR filter enabled. Coefficients [57,92,–279,21,704,–720,–1163,4127,10784]/2^14

Table 2 Clock generator

Parameter	Condition	Unit	Min	Typical	Max
Internal clock reference					
Frequency		MHz		10	
Accuracy		ppm		±3 ±1/year	
Internal sampling clock generator [5]					
Frequency range 1	4-channel mode	MHz	2440	2500	2500
Frequency range 2	4-channel mode	MHz	1473		1627
Frequency range 1	2-channel mode	MHz	4880	5000	5000
Frequency range 2	2-channel mode	MHz	2946		3254
External clock reference input (front panel CLK connector)[6]					
Frequency		MHz	1	10	500
Frequency [7]	Jitter cleaner enabled	MHz	10 -10 ppm	10	500 +10 ppm
Frequency	Delay line used	MHz		10	100
Delay line tuning range		ps		500	
Signal level	Recommended	Vpp	0.5		3.3
Input impedance	AC	Ω		50	
Input impedance	DC	Ω		10k	
Input impedance (high) [8]	AC	Ω		200	
Clock reference output (front panel CLK connector)[9]					
Frequency		MHz		10	
Signal level	Into 50-Ω load	Vpp		1.2	
Output impedance	AC	Ω		50	
Output impedance	DC	Ω		10k	
External direct sampling clock input (front panel CLK connector)[10]					
Frequency [11]		MHz	1000	2500	2500
Signal level	Recommended	Vpp	0.5		3.3
Impedance	AC	Ω		50	
Impedance	DC	Ω		10k	

[5] The internal clock generator can generate frequencies in two different ranges.
[6] Use clock reference from an external source to synchronize the ADQ36 to the external source.
[7] The jitter cleaner requires the reference frequency to be a multiple of 10 MHz within ± 10ppm.
[8] Software-selectable high-impedance mode.
[9] For using the ADQ36 as the master for synchronizing other equipment.
[10] Use an external clock. Bypass the internal clock generator. Use typical 2500 MHz for both 2-channel and 4-channel mode.
[11] In two-channel mode, the sampling frequency is twice the external clock frequency.

Table 3 Front panel TRIG connector

Parameter	Condition	Unit	Min	Typical	Max
Used as input					
Impedance	DC	Ω		50	
Impedance (high) [12]	DC	Ω		500	
Signal level	50-Ω mode	V	-0.5		3.3
Adjustable threshold	50-Ω mode	V	0		2.8
Signal level	High impedance	V	-0.5		5.5
Adjustable threshold	High impedance	V	0		2.3
Pulse repetition frequency		MHz			10
Time resolution [13]	As trigger	ps		50	
Update rate [13]	As GPIO	MHz			156.25
Used as output					
Impedance	DC	Ω		50	
Output level high	Into 50-Ω load	V	1.4		
Output level high[14]	Unterminated	V	3.1		
Output level low	Into 50-Ω load	V			0.1
Pulse repetition frequency [13]		MHz			156.25

Table 4 Front panel SYNC connector (SYNC is a trigger signal with limited timing resolution)

Parameter	Condition	Unit	Min	Typical	Max
Used as input					
Impedance	DC	Ω		50	
Impedance (high) [12]	DC	Ω		500	
Signal range	50-Ω mode	V	-0.5		3.3
Adjustable threshold	50-Ω mode	V	0		2.8
Signal level	High impedance	V	-0.5		5.5
Adjustable threshold	High impedance	V	0		2.3
Pulse repetition frequency	As trigger	MHz			10
Time resolution [13]	As trigger	ns		3.2	
Update rate [13]	As GPIO	MHz			156.25
Used as output					
Impedance	DC	Ω		50	
Output level high	Into 50-Ω load	V	1.4		
Output level high	Unterminated	V	3.1		
Output level low	Into 50-Ω load	V			0.1
Pulse repetition frequency [13]		MHz			156.25

[12] Software-selectable high-impedance mode
[13] Timing properties are valid for 2.5 GSPS and 5 GSPS and scale linearly with sampling frequency.
[14] Driving an unterminated 50-ohm line with the output gives good signal integrity and high swing at the far end since the output provides proper source termination

Table 5 Front panel GPIO connector

Parameter	Condition	Unit	Min	Typical	Max
Single-ended GPIO signals					
Number of signals				12	
Input level high		V	2		
Input level low		V			0.8
Output level high	100 uA	V	3.1		
Output level low	100 uA	V			0.1
Output level high	8 mA	V	2.5		
Output level low	8 mA	V			0.6
Update rate per pin		Mbit/s			156.25
Differential LVDS signals					
Number of inputs				4	
Number of outputs				3	
Update rate per pin		Mbit/s			156.25

Table 6 Environment and mechanical parameters

Parameter	Condition	Unit	Min	Typical	Max
Power and temperature					
Power consumption		W		60	
Power supply		V	10.8	12	13.2
Operating temperature		°C	0		45
Size					
Width		slots		2	
Height		mm		3U	
Mechanical standard				PXIe Type 2	
Compliances					
RoHS3				Yes	
CE				Yes	
FCC	Exclusion according to CFR 47, part 15, paragraph 15.103(c)				

Table 7 Data Acquisition

Parameter	Condition	Unit	Min	Typical	Max
Re-arm time		ns			20
Acquisition memory (Data FIFO)	Shared by all channels	GiBytes		8	
Record length		samples	1		2^{31}
Pre-trigger		samples	0		16 360
Trigger delay	4-channels mode	samples	0		2^{35}-8
Length granularity pre-trigger and trigger delay	4-channels mode	samples	8		
Trigger delay	2-channels mode	samples	0		2^{36}-16
Length granularity pre-trigger and trigger delay	2-channels mode	samples	16		

Table 8 Data Transfer

Parameter	Unit	Value
Supported PCIe versions		Gen1 Gen2 Gen3
Supported number of lanes		1 4 8
Sustained data rate to CPU, with headers	GByte/s	5
Sustained data rate to CPU, without headers	GByte/s	7
Sustained data rate to GPU, without headers	GByte/s	7
Sustained data rate peer-to-peer to GPU, without headers	GByte/s	7

Table 9 Software support

Parameter	Value
Operating system[15]	Windows 10 Linux
GUI	Digitizer Studio
Example code	C, Python
API[16]	C / C++

[15] See the document 15-1494 for a listing of supported distributions.
[16] Note that only the C / C++ interface enables maximum data transfer rate.

3 FEATURES FOR DATA FLOW CONTROL, SYNCHRONIZATION AND PROCESSING

The ADQ36 features advanced machinery for flow control, synchronization, and signal processing. The block diagrams are shown in Figure 1 and Figure 2. The features are described in the following tables.

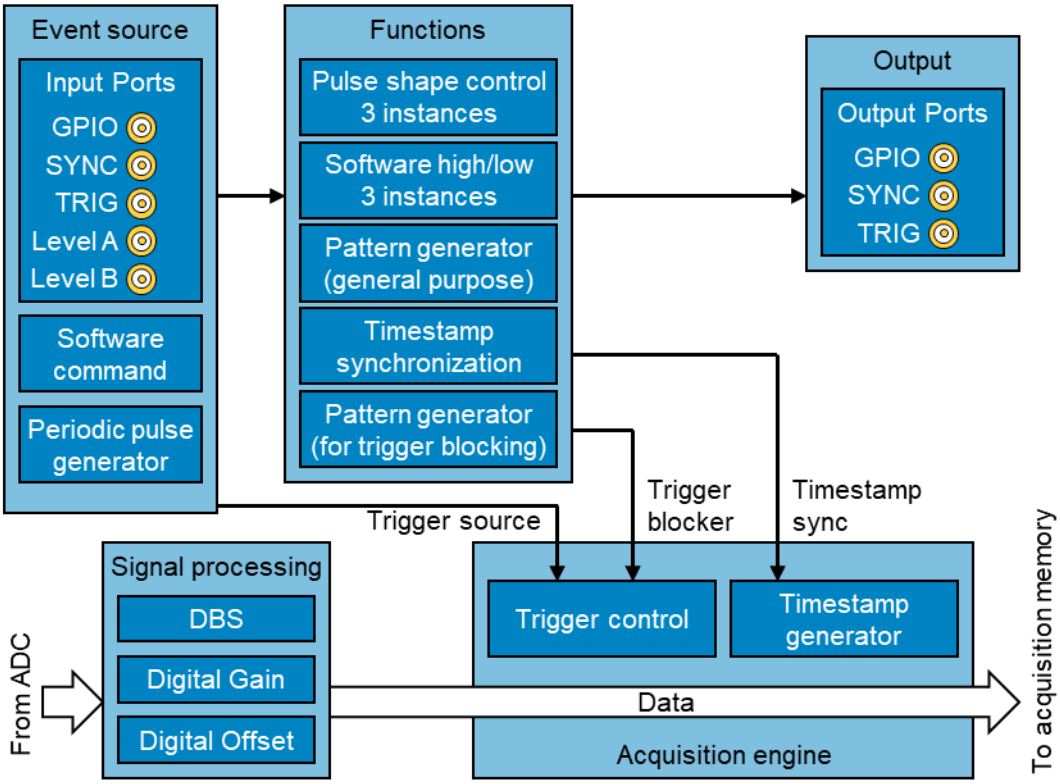


Figure 1 Flow control and synchronization block diagram

Table 10 Digital signal processing blocks

Object type	Available features
Digital Signal Processing Included signal processing in the data path for enhanced signal quality	Digital Baseline Stabilizer (DBS) Digital gain Digital offset Programmable FIR filter

Table 11 Flow control blocks

Object type	Available features
Input ports Electrical connections to the ADQ36 for real-time operation (excluding the PCIe data interface). Used as event source.	Front panel TRIG Front panel SYNC Front panel GPIO Front panel CLK (clock reference or clock input only) Analog channel A Analog channel B Analog channel C Analog channel D
Event sources Signals for real-time control of activities in the firmware of ADQ36	Software command External TRIG External SYNC External GPIO Internal periodic event generator Level analog channel A Level analog channel B Level analog channel C Level analog channel D
Functions Included operations for real-time control of activities in the firmware of ADQ36	Pattern generator for timestamp synchronization General purpose pattern generator, 2 instances Pulse generator, 4 instances
Output ports Electrical connections to the ADQ36 for real-time operation (excluding the PXIe data interface)	Front panel TRIG Front panel SYNC Front panel GPIO Front panel CLK (clock reference output only)

Table 12 Firmware Functions for flow control

Function	Modes / Selections	Event Sources as stimuli
Pattern generator for timestamp sync Control the time of the ADQ36		Software command External TRIG External SYNC Internal periodic event generator
Pulse generator Control output pulse shapes. Three instances.	Rising edge Falling edge Pulse length Polarity	Software command External TRIG External SYNC Internal periodic event generator
Pattern generator for trigger blocking	Once Window Gate Trigger counter	Software command External TRIG External SYNC Internal periodic event generator

Table 13 Firmware functions for acquisition

Function	Modes	Event Sources as stimuli
Trigger Start the acquisition of a data record		Software command External TRIG External SYNC Internal periodic event generator Level analog channel A Level analog channel B Level analog channel C Level analog channel D
Data acquisition modes Configurations for sending digital data to the host PC	Streaming with header Streaming without header	

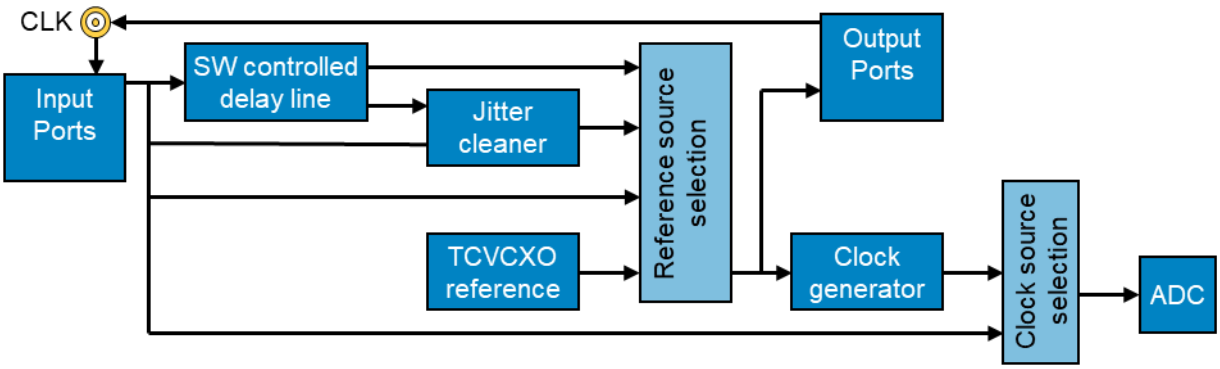
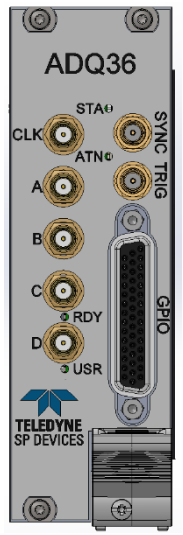


Figure 2 Clock generation block diagram

Table 14 Clock generation

Function	Modes
Clock reference source Phase and frequency reference for the clock system	Internal External External with jitter cleaner and/or delay-line
Sampling clock sources Actual clock for taking the samples of the analog data	Internal clock generator Direct external clock
Clock output	Selected clock reference

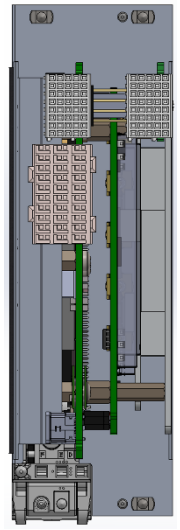
4 FRONT PANEL CONNECTORS AND LEDS



CLK	SMA	Clock reference in/out. Direct clock
A	SMA	Analog channel A
B	SMA	Analog channel B (used in 2-channel mode)
C	SMA	Analog channel C
D	SMA	Analog channel D (used in 2-channel mode)
STA	Multi-color LED	Status
ATN	LED	PXIe attention
RDY	Green LED	Ready
USR	Blue LED	User / Start-up
SYNC	SMA	External trigger and synchronization
TRIG	SMA	External trigger
GPIO	HD-DSUB 44	General purpose input/output

5 PXIE BACKPLANE CONNECTORS

The ADQ36-PXIe requires two slots in the PXIe chassis. The connector in the leftmost slot is only used to supply additional power to the digitizer.



PCIe	Slot 1	Generation 3 by 8 lanes
Power	Slot 1	12V
PXIe_DStarA	Slot 1	Star trigger clock (not used)
PXIe_DStarB	Slot 1	Star trigger to ADQ36
PXIe_DStarC	Slot 1	Star trigger from ADQ36
PXIe clk100	Slot 1	Backplane clock reference
PXIe sync100	Slot 1	Backplane clock reference
PXI_Trig0	Slot 1	Available for future use
PXI_Trig1	Slot 1	Available for future use
GA0-5	Slot 1	Available for future use
SMB	Slot 1	Available for future use
Power	Slot 2	Additional power 12 V

Figure 3 PXIe backplane connectors.

6 CONFIGURING NUMBER OF CHANNELS

Changing from 4-channel mode to 2-channel mode is done by changing firmware image in the FPGA. Both firmware images are available in a non-volatile memory on the ADQ36 digitizer. The software tool ADQAssist can be used to change which firmware image will be loaded into the FPGA the next time the ADQ36 is reset. Changing firmware requires power cycling of the PC for the PCIe bus to enumerate.

The analog input connectors for Channel B and D are used in the 2-channel mode.

7 ABSLOUTE MAXIMUM RATINGS

Table 15 Absolute maximum ratings

Parameter	Condition	Unit	Min	Max
Power supply to GND		[V]	-0.4	14
Temperature operation		[°C]	0	45
Analog in to GND		[V]	-1.75	+1.75
TRIG to GND	50-Ω mode	V	-2	5
SYNC to GND	50-Ω mode	V	-2	5
TRIG to GND	500-Ω mode	V	-2	6
SYNC to GND	500-Ω mode	V	-2	6
CLK REF to GND AC amplitude		[Vpp]		5
CLK REF to GND DC level		[V]	-5	5
GPIO to GND		[V]	-1.5	5

Exposure to conditions exceeding the absolute maximum ratings may reduce lifetime or permanently damage the device. The built-in temperature monitoring unit will protect the digitizer from overheating by temporarily shutting down parts of the device in an overheat situation.

The SMA connectors have an expected lifetime of 500 operations. For frequent connecting and disconnecting of cables, connector savers are recommended.

8 TYPICAL PERFORMANCE

8.1 Frequency response

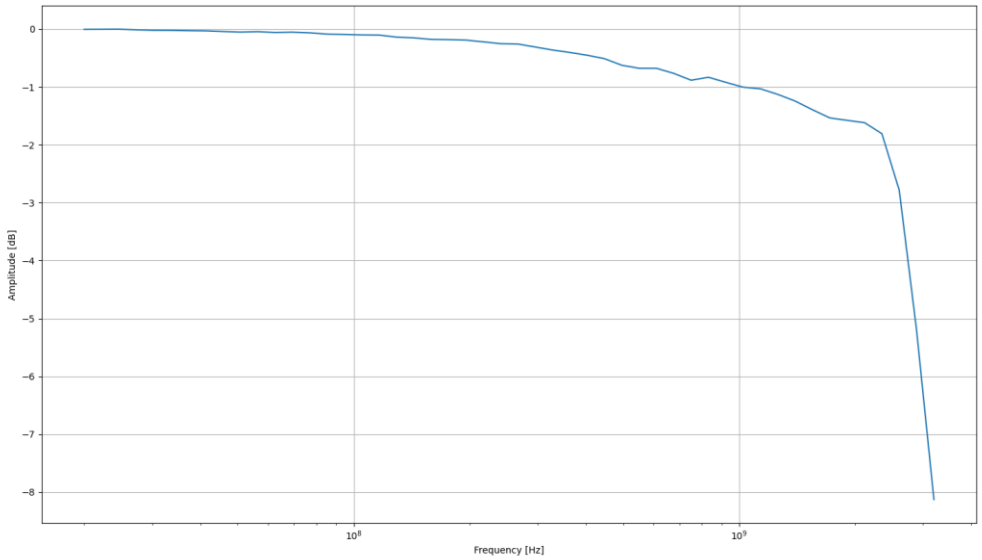


Figure 4 Typical frequency response

8.2 Crosstalk

Figure 5 Typical crosstalk in 4-channel mode. Channel A to B, C and D.

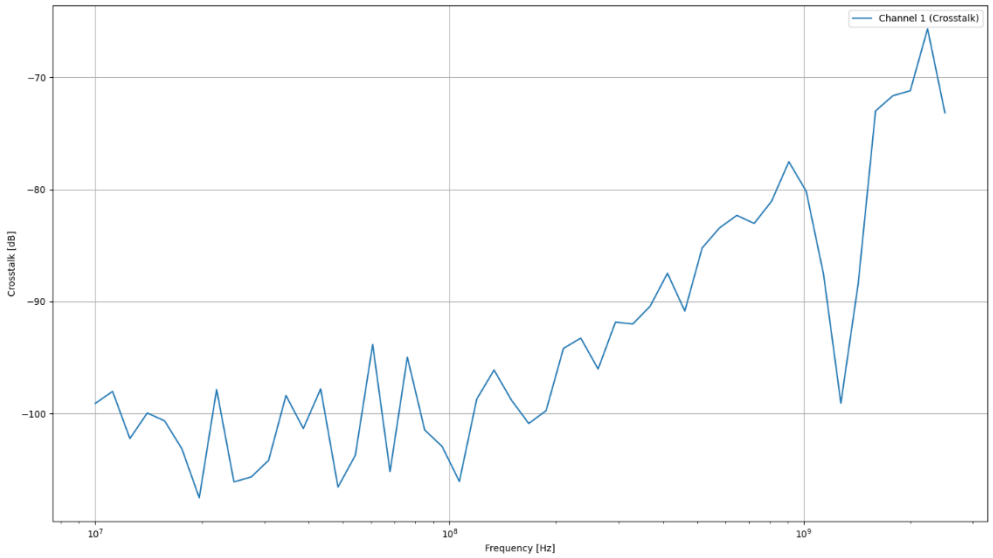


Figure 6 Typical crosstalk in 2-channel mode.

8.3 Frequency domain 4-channel mode

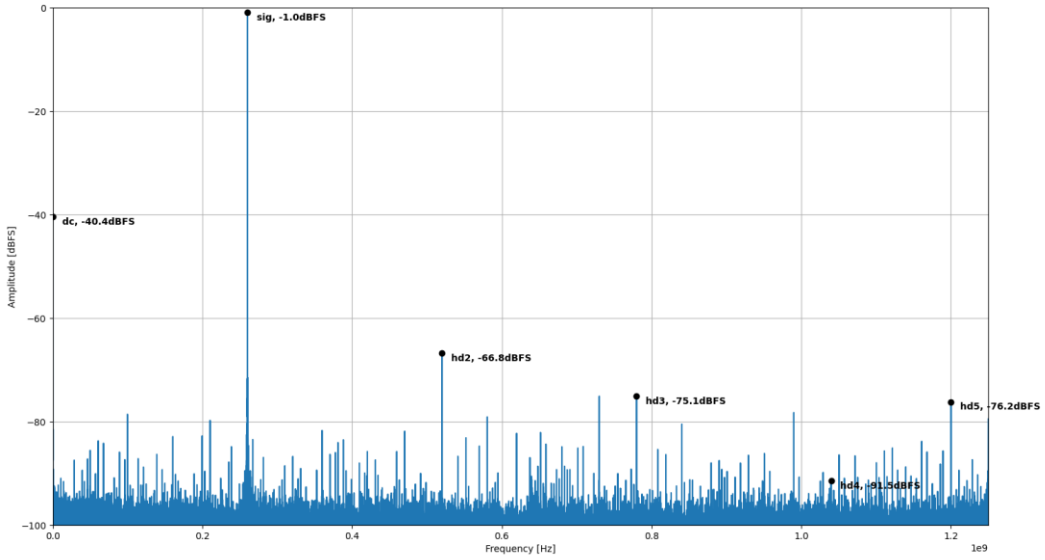


Figure 7 FFT typical single tone performance, 4-channel mode at 2.5 GSPS

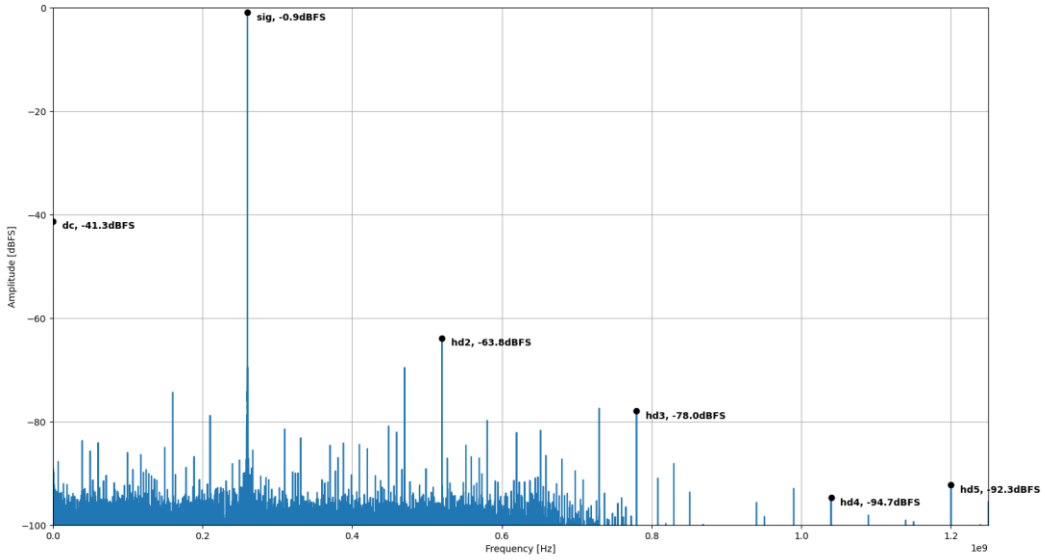


Figure 8 FFT using built in programmable FIR, 4-channel mode at 2.5 GSPS

8.4 Frequency domain 2-channel mode

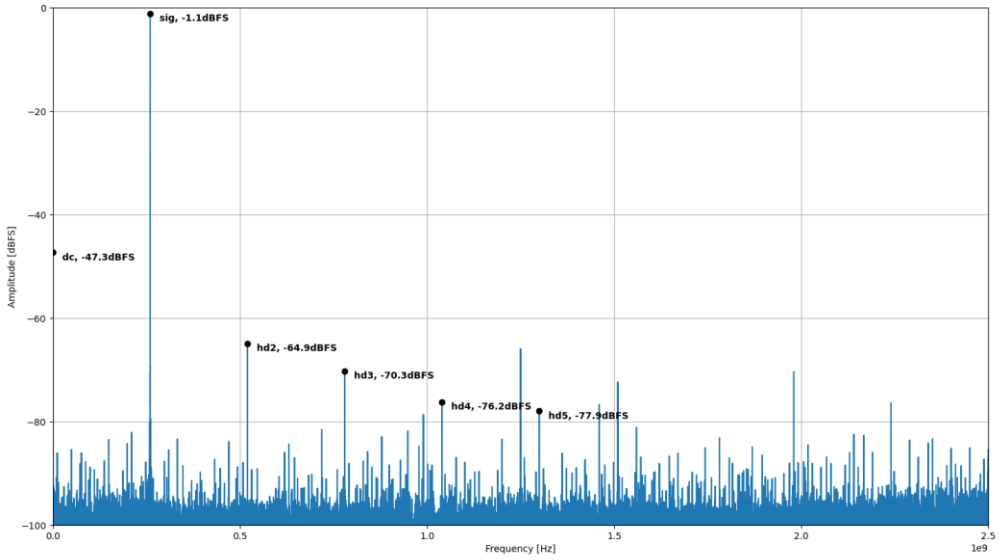


Figure 9 FFT typical single tone performance, 2-channel mode at 5 GSPS

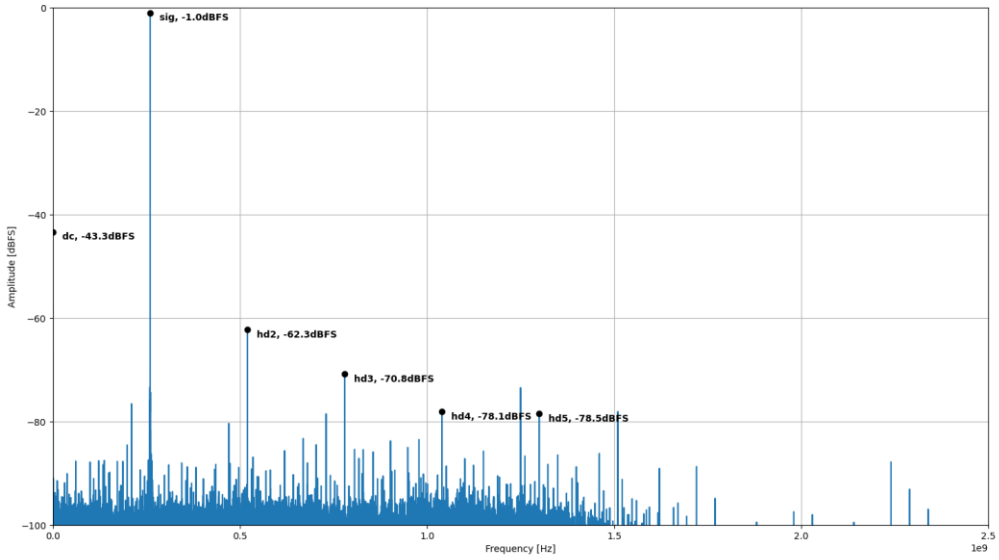


Figure 10 FFT using built in programmable FIR, 2-channel mode at 5 GSPS

9 BLOCK DIAGRAM

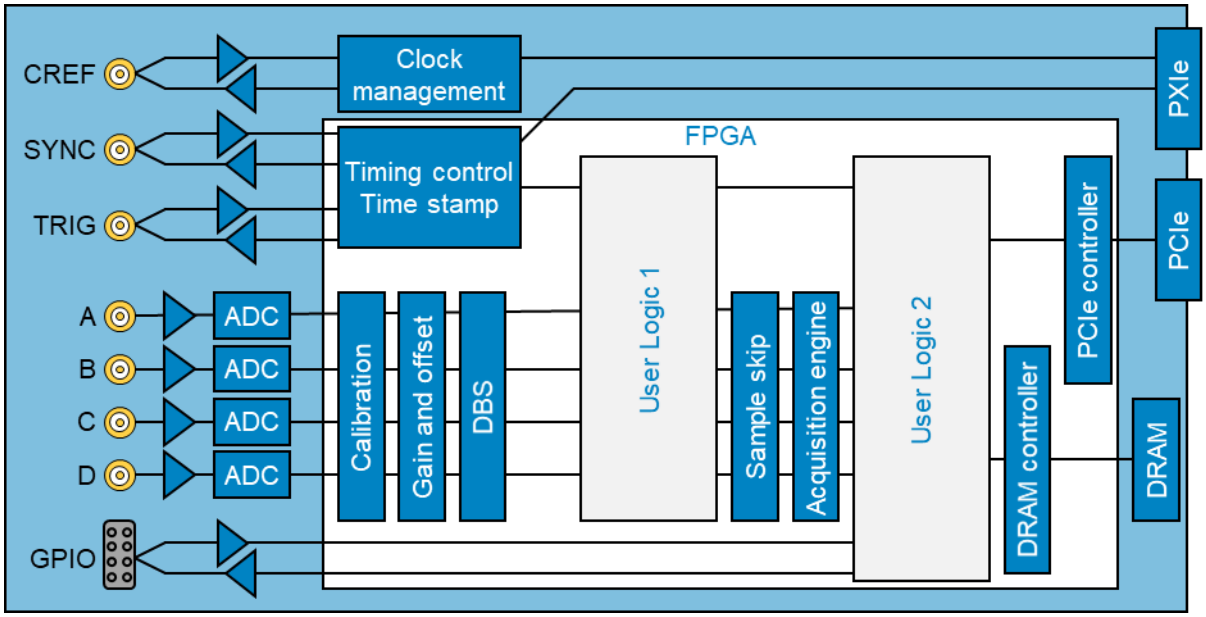


Figure 11 Block diagram of ADQ36-PXIe

Figure 12 ADQ36-PXIe

Important Information

Teledyne Signal Processing Devices Sweden AB (Teledyne SP Devices) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to Teledyne SP Devices' general terms and conditions supplied at the time of order acknowledgment.

Teledyne SP Devices warrants that each product will be free of defects in materials and workmanship, and conform to specifications set forth in published data sheets, for a period of three (3) years. The warranty commences on the date the product is shipped by Teledyne SP Devices. Teledyne SP Devices' sole liability and responsibility under this warranty is to repair or replace any product which is returned to it by Buyer and which Teledyne SP Devices determines does not conform to the warranty. Product returned to Teledyne SP Devices for warranty service will be shipped to Teledyne SP Devices at Buyer's expense and will be returned to Buyer at Teledyne SP Devices' expense. Teledyne SP Devices will have no obligation under this warranty for any products which (i) has been improperly installed; (ii) has been used other than as recommended in Teledyne SP Devices' installation or operation instructions or specifications; or (iii) has been repaired, altered or modified by entities other than Teledyne SP Devices. The warranty of replacement products shall terminate with the warranty of the product. Buyer shall not return any products for any reason without the prior written authorization of Teledyne SP Devices.

In no event shall Teledyne SP Devices be liable for any damages arising out of or related to this document or the information contained in it.

TELEDYNE SP DEVICES' EXPRESS WARRANTY TO BUYER CONSTITUTES TELEDYNE SP DEVICES' SOLE LIABILITY AND THE BUYER'S SOLE REMEDY WITH RESPECT TO THE PRODUCTS AND IS IN LIEU OF ALL OTHER WARRANTIES, LIABILITIES AND REMEDIES. EXCEPT AS THUS PROVIDED, TELEDYNE SP DEVICES DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING ANY WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT.

TELEDYNE SP DEVICES DOES NOT INDEMNIFY, NOR HOLD THE BUYER HARMLESS, AGAINST ANY LIABILITIES, LOSSES, DAMAGES AND EXPENSES (INCLUDING ATTORNEY'S FEES) RELATING TO ANY CLAIMS WHATSOEVER. IN NO EVENT SHALL TELEDYNE SP DEVICES BE LIABLE FOR SPECIAL, INCIDENTAL OR CONSEQUENTIAL DAMAGES, INCLUDING LOST PROFIT, LOST DATA AND THE LIKE, DUE TO ANY CAUSE WHATSOEVER. NO SUIT OR ACTION SHALL BE BROUGHT AGAINST TELEDYNE SP DEVICES MORE THAN ONE YEAR AFTER THE RELATED CAUSE OF ACTION HAS ACCRUED. IN NO EVENT SHALL THE ACCRUED TOTAL LIABILITY OF TELEDYNE SP DEVICES FROM ANY LAWSUIT, CLAIM, WARRANTY OR INDEMNITY EXCEED THE AGGREGATE SUM PAID TO SP BY BUYER UNDER THE ORDER THAT GIVES RISE TO SUCH LAWSUIT, CLAIM, WARRANTY OR INDEMNITY.

Worldwide Sales and Technical Support

www.spdevices.com

Teledyne SP Devices Corporate Headquarters

Teknikringen 6
SE-583 30 Linköping
Sweden

Phone: +46 (0)13 465 0600
Fax: +46 (0)13 991 3044
Email: info@spdevices.com