



## Application Note: Clocking

*The ADQ series of digitizers has an advanced clock system for flexible synchronization to external equipment. This document is a general description of the clock system. It also contains examples on how to use the clock system.*

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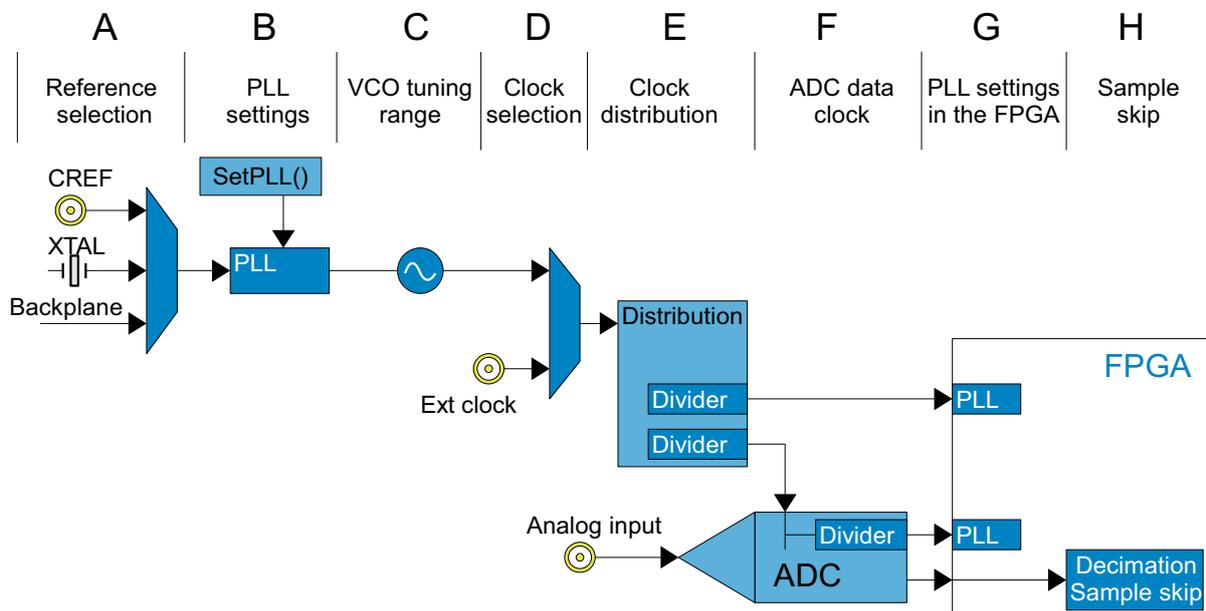
## 1 Introduction

The ADQ series of digitizers has clock reference and internal clock source as well as a connector for direct external clock. The intention with the clock design is to synchronize several different hardware units. The clocking system has a lot of flexibility. It also has a lot of limitations. The application note intend to give understanding on how the clocking works and why there are limitations.<sup>1</sup>

A typical situation where this application note is useful is when the signal source has a clock reference and the digitizer should be synchronized to that source. Many instruments use 10 MHz. Then it is straight forward. However, for other reference frequencies, the clock network has to be controlled in several nodes, which are described here.

## 2 Clock architecture

The clock architecture is in **Figure 1**. The different nodes are listed in **Table 1**.



**Figure 1: Clock architecture**

1. The description is general. Deviations and limitations are different on the different ADQ digitizer models.

#	NAME	DESCRIPTION	ENABLES	PARAMETERS	BOUNDARIES
A	Reference selection	Select internal clock reference source.	Synchronization of several digitizers and trigger.	External Internal XTAL Backplane ref	Frequency range
B	PLL setting	Set the ratio between the internal VCO and the selected reference.	Select best reference frequency for the system.	R divider N divider VCO divider	Allowed settings
C	VCO tuning range	Set the frequency of the internal VCO and indirectly the sampling frequency.	Fine tuning of sampling frequency	VCO frequency	Tuning range
D	Clock selection	Select clock source	Synchronization	Internal External	Frequency range
E	Clock distribution	Generate internal clock frequencies from the clock source.	Optimized clock rate for the different parts of the system.	VCO divider	Allowed settings
F	ADC data clock	The ADC data clock is derived from the sampling clock	Communication with FPGA	Set by design	N/A
G	PLL settings in the FPGA	Generate internal clocks from data clock and system clock.	Internal sampling frequency	Set by design	N/A
H	Decimation / Sample skip	Reduce data rate by decimation or sample skip	Reducing sampling frequency	Reduction Ratio	Allowed settings

**Table 1: Clock blocks**

### 3 Description of the blocks

#### 3.1 Reference selection

The first step is to select a clock reference source (unless direct external clock is used, [Section 3.4](#)). There are several sources available to meet various requirements on synchronization.

The default PLL settings are for a clock reference frequency of 10 MHz. If another reference frequency is required, use SetPLL() command to get the correct sampling clock frequency, see [Section 3.2](#) and [Section 7.1](#).

REFERENCE SOURCE	PARAMETERS	PURPOSE	AVAILABLE	
			ADQ V5	ADQ V6
Built in TCXO	10 MHz	Stand alone operation	All	All
External reference	1 – 250 MHz	External master	All	All
Backplane	1 – 250 MHz	Chassis system	–	PXIe / MTCA

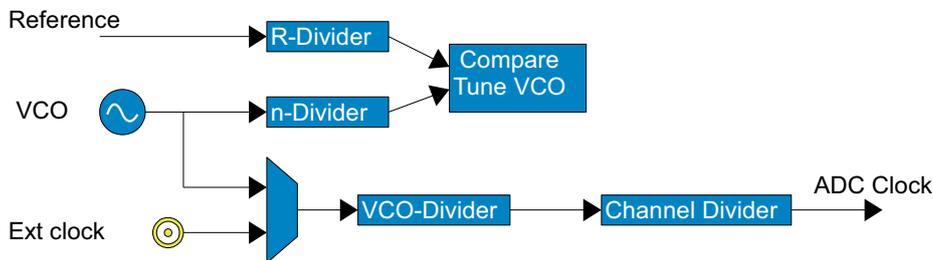
**Table 2: Clock reference sources**

#### 3.2 PLL setting

The ADQAPI command SetPLL() gives full access to the divider settings in the PLL. See ADQAPI Users guide on how to use SetPLL(). [Figure 2](#) illustrates the dividers, that is, the parameters in the SetPLL() command.

PARAMETER	ADQ V5 DESCRIPTION	PARAMETER	ADQ V6 DESCRIPTION	PARAMETER
N-divider	Set compare frequency	VCO: <a href="#">Table 4</a> $N = VCO * R / f_{ref}$	Set compare frequency	VCO: <a href="#">Table 4</a> $N = VCO * R / f_{ref}$
R-divider	Set compare frequency	$f_{ref} / R < 100$ $1 M < f_{ref} < 250 M$	Set compare frequency	$f_{ref} / R < 100$ $1 M < f_{ref} < 250 M$
VCO divider	Set clock frequency	2,3 ... 20	Set by API. Not available for user	–
Channel divider	Set by API. Not available for user	–	Set by API. Not available for user	–

**Table 3: SetPLL() parameters**



**Figure 2: Dividers in the PLL which are controlled by the SetPLL() command.**

### 3.3 VCO tuning

The internal VCO has a limited tuning range. It is typically +/- 10% of the center frequency. Note that the VCO frequency is not the same as the sampling frequency. In some models, there is a divider between the VCO and the clock to the ADC. When changing the PLL settings and reference frequency, care has to be taken so that the VCO is within its tuning range.

### 3.4 Clock Selection

Select the internal clock or a direct external clock source. The external clock source is then a direct sampling clock. Note that on some interleaved digitizers a different ratio is valid, see [Section 3.6](#) and [Table 4](#).

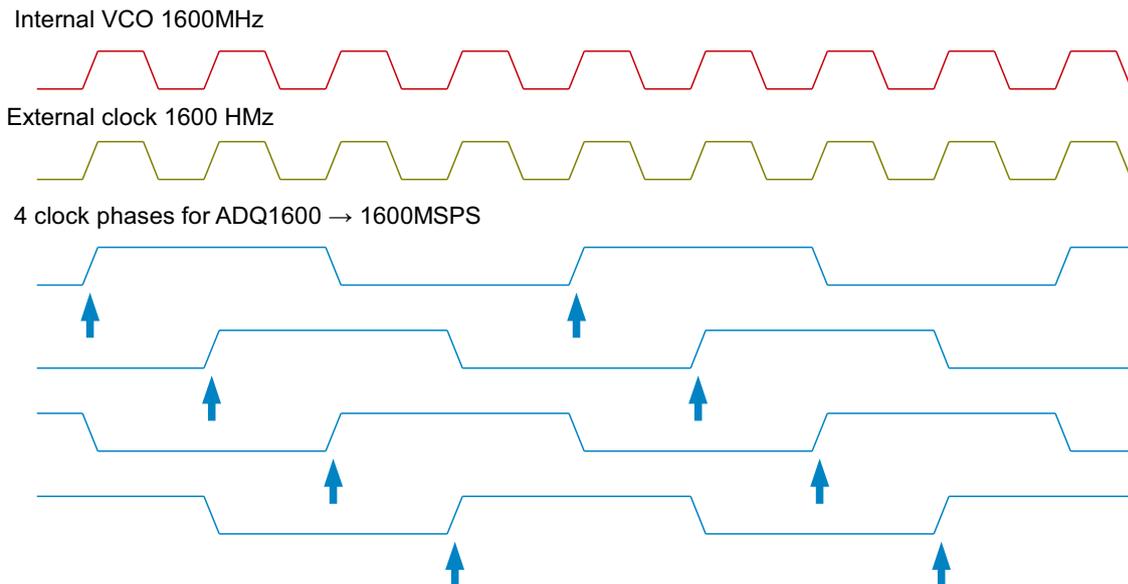
### 3.5 Clock distribution

Different parts of the digitizer requires different clocks. There is a clock distribution network with clock dividers on the digitizer. The ADC clock is from one branch in this distribution. The clock divider is phase locked to the reference on ADQ V6. This is not the case for ADQ V5, see [Section 4.5](#).

### 3.6 External clock for interleaved digitizers.

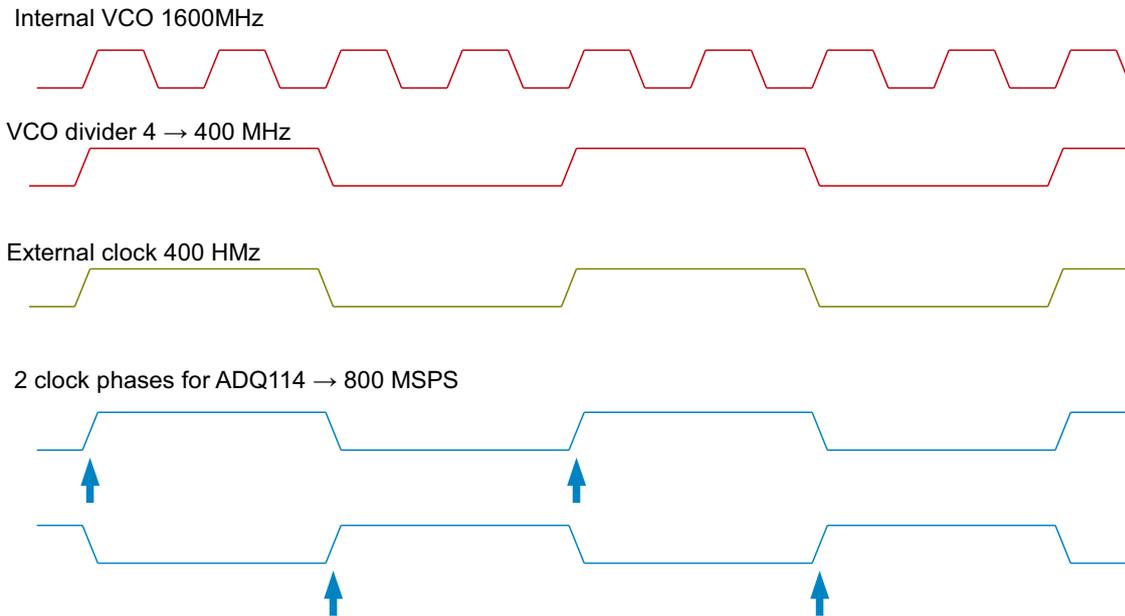
The clock for the interleaved ADCs can be generated in different ways. This result in that the ratio between an external clock and the sample rate of is different for the different digitizer models.

One method is that the clock for the interleaved digitizers is generated a divider in different phases of a base clock. This is illustrated for ADQ1600 in **Figure 3**. This method implies that also an external clock should run at the sampling frequency.



**Figure 3: Clock phases on interleaved ADQ1600**

The other method is to generate the interleaving clock as clock and inverse of the clock. This gives an interleaving of a factor of 2. In this way a 400MHz external clock generates 800 MSPS, **Figure 4**.



**Figure 4: Clock phases on interleaved ADQ114**

Yet another way is to generate the phases from the fundamental clock. A 1.75 GHz clock in to the ADQ108 is set up to generate 4 phases and thus 7 GSPS.

On SDR14, the external clock has to be 2X the sampling frequency because of the AWG update rate.

### 3.7 ADC data clock

Data out from the ADC has a data clock for synchronizing with the data input in the FPGA. This clock is derived from the sampling clock in a divider. When changing the sampling clock frequency, this clock will also change. This may affect the timing of data in to the FPGA.

The ADC data clock rate is not of interest for the user in normal operation, but it is important when using the ADQ Development Kit for developing custom firmware.

### 3.8 PLLs in the FPGA

Some parts of the FPGA has to run synchronous to the data clock in order to maintain the data rate. There are PLLs that regenerate internal clocks from the data clock. Since the data clock is derived from the sampling frequency, changing sampling frequency will have an impact on the PLLs in the FPGA. The frequency range for these PLLs is very limited. Therefore the number of settings on the sampling frequency is limited.

In ADQ V5 there is a low frequency mode and a high frequency mode which set different parameters to these PLLs. When the internal clock frequency is changed, these settings are selected automatically. But when using an external clock, the settings has to be selected by the SetClockFrequencyMode() command.

SDR14 contains ADCs for the acquisition, DACs for signal generation and an advanced trigger synchronization. Changing the clock frequency would interfere the timing between these parts and synchronism on the digitizer cannot be maintained. Therefore SDR14 only allows limited tuning around the specified clock frequency.

### 3.9 Sample skip<sup>1</sup>

The data rate can be reduced by changing the clock rate to the ADC. However, this affects a lot of parts in the system. An alternative is to reduce the data rate in the FPGA by discarding samples. This is the sample skip function. For example, setting sample skip to 2 will save every second sample. This is the same as reducing the sample rate by a factor of 2. See ADQ API users guide for more details.

See [Table 5](#) and [Table 6](#) for frequency listing on ADQ412.

### 3.10 Decimation

Decimation is sample skip preceded by a low pass filter for noise reduction. Decimation is available on ADQ214<sup>2</sup>.

## 4 Synchronizing several digitizers

### 4.1 Background

To build a system with many channels, several digitizers are needed. These has to be synchronized. There are several parameters in the measurement set up that calls for different solutions. Synchronization is also necessary for sample precise triggering of a large number of channels.

### 4.2 Straight forward free running operation

The internal clock of the digitizers is extremely accurate. The deviation from the nominal frequency is in the order of a few ppm. In many situations this is enough. With an external trigger and only a few kilo samples per record this straight forward solution may be good enough.

### 4.3 Common clock reference

Although the internal clock accuracy is a few ppm, this deviation can build up to several samples in the end of long records (record length 100 kSamples). In a system with several digitizers, the deviation between channels may be significant. In this case a common clock reference may lock the frequencies in the different devices to each other.

A common clock reference is also crucial for the time stamp function, which counts sample clock periods from a certain time point. Drifting clocks may result in differences in the time stamp counters. This is solved with a common clock reference.

There is a clock reference input on the front panel.

For PXIe and MTCA formats, a clock reference from the backplane may be used.

On ADQ V6, there is a clock reference output which can be used as clock reference input of a to a second card.

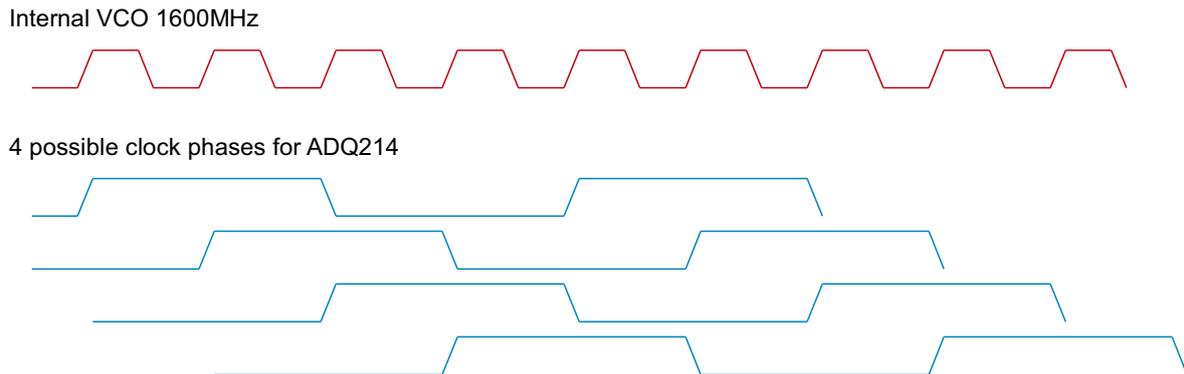
### 4.4 Direct external clock.

The direct clock input is available for synchronization of systems where a sample clock i already available. It gives no direct advantages over a reference distribution except on the ADQ V5 products, see [Section 4.5](#).

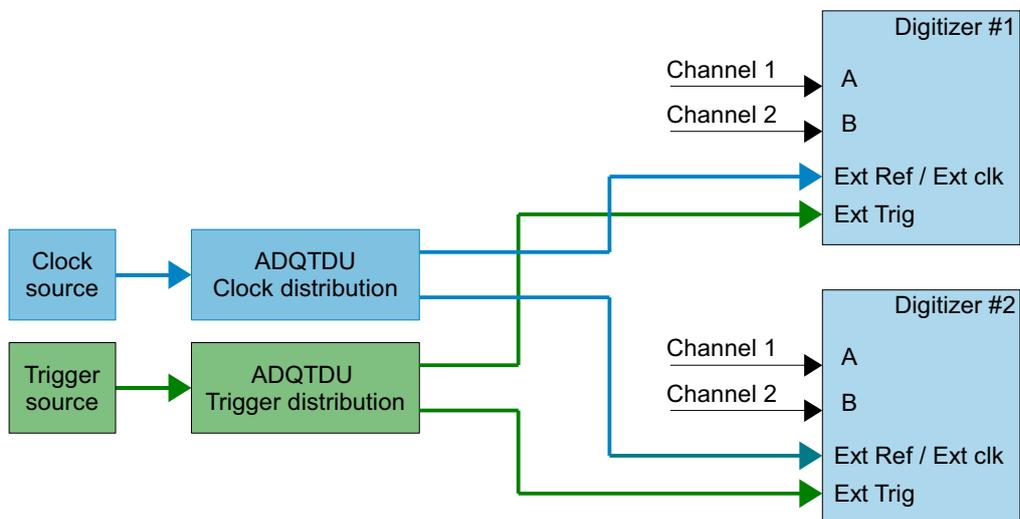
- 
1. Contact an SP Devices' sales representative for information on which digitizers that support sample skip
  2. Contact an SP Devices' sales representative for information on decimation option for other digitizers.

#### 4.5 Clock distribution ADQ V5 only

On ADQ V5, the VCO divider is not phase locked to the reference. Therefore, the sampling clock phase may vary from start-up to start-up, **Figure 5**. This is normally not an issue. But if the synchronism is required, it can be handled by using an external clock source or by the extended trigger accuracy (see trigger application note). For larger systems with several digitizers, the ADQTDU can do clock distribution and trigger distribution, **Figure 6**. See datasheet of ADQTDU for more information.



**Figure 5: Clock phases on ADQ V5**



**Figure 6: Using ADQTDU for synchronized operation on ADQ V5.**

## 5 Setting frequency in ADCaptureLab

On ADQ V5 digitizers, setting clock frequency in ADCaptureLab will change the dividers in the clock distribution. Since the divider is an integer, the number of available frequencies are limited.

On ADQ V6 digitizers, setting the clock frequency changes the PLL dividers.

## 6 Clock jitter and phase noise

There are 2 types of clock uncertainty; jitter and phase noise.

If the internal clock generator is used, The digitizer will be subject to phase noise. This is typically the integral of a Gaussian stochastic process. The result is a widening of the signal, a skirt in the frequency domain.

The other clock uncertainty is jitter. When the frequency is locked to a fixed reference, each clock edge is an independent Gaussian process. The result is a flat noise floor. This jitter is translated to noise by the model

$$\text{SNR} = 20 \log_{10} (1 / (2 \pi f t)) \quad (1)$$

The ADQ412 has an SNR of 49 dB at 2 GHz. This yields 280 fs RMS jitter. The noise is frequency dependent. It has to be measured at a high frequency,

## 7 Examples

### 7.1 Synchronizing to an external equipment

It is possible to use the external clock reference to synchronize to an external equipment. If the external equipment has a 10 MHz reference, this is straight forward. But not all systems are based on multiples of 10 MHz. Synchronizing to these systems requires frequency planning and tuning of the digitizer clock system.

Using, for example, a 30.72 MHz clock reference on an ADQ1600 is possible. The VCO tuning range is 1400–1800. Using r-divider = 1 and n-divider = 48 gives a VCO frequency of 1.4746 GHz. The sample rate is then 1.4746 GHz.

### 7.2 Setting clock frequency

The VCO of ADQ214 has a tuning range from 1400 to 1800 MHz with a nominal frequency of 1600 MHz. The sampling frequency is set in the clock divider. The clock divider can do

$$\text{VCO\_frequency} / 2 / N \text{ where } N \text{ is } 2, 3, 4, 5, \dots \quad (2)$$

The frequencies are nominal 400, 266.7, 200 ... MHz. Assume that the PLL settings are fixed and that the external reference is tuned up and down from a nominal 10 MHz. The PLL divider ratio is found as

$$\text{VCO\_frequency} / \text{Reference\_frequency} = 1600 / 10 = 160 \quad (3)$$

The VCO tuning range gives a limit on the clock reference range as

$$\begin{aligned} [ 1400 / 160 = 8.75 \\ 1800 / 160 = 11.25 ] \end{aligned} \quad (4)$$

The available sampling frequencies over the tuning range are then for N=2:

$$[ 1400 / 2 / 2 = 350 \\ 400 ] \text{ (limited by ADC spec)} \quad (5)$$

For N=3, the range is

$$[ 1400 / 2 / 3 = 233.3 \\ 1800/2/3 = 300 ] \quad (6)$$

and so on. Note that there is a gap between 300 MHz and 350 MHz which cannot be reached. This range can only be accessed with external clock.

Instead of tuning the external reference frequency, it is possible to tune the PLL divider ratio and get the similar result. The sampling frequencies will then be in the same range, but set in discrete steps.

## 8 Clock frequency ranges.

### 8.1 Parameters

There are sets of clock frequency ranges for each digitizer. **Table 4** summarizes settings on the different digitizers.

MODEL	VCO [GHZ] <sup>1</sup>	FS	CLOCK FREQUENCIES <sup>2</sup>	N <sup>3</sup>	EXT CLK	SAMPLE SKIP
ADQ114	1.4 – 1.8	0.8	–	2 – 20	0.4	1 2 4 8 12 16 ...
ADQ214	1.4 – 1.8	0.4	–	2 – 20	0.4	1 2 4 8 12 16 ...
ADQ108	1.4 – 1.8	7	7 6.5 6	–	1.75	1 2 4 8 16 32 64 128
ADQ412	1.72 – 2.25	1 / 2	[1000 950 900 860] / [2000 1900 1800 1720]	–	1 – 0.86/ 1 – 0.86	1 2 4 8 16 32 64 128
ADQ412–3G	1.4 – 1.8	1.8 / 3.6	[1800 1700 1600 1500 1400] / [3600 3400 3200 3000 2800]	–	1.8 – 1.4/ 1.8 – 1.4	1 2 4 8 16 32 64 128
ADQ412–4G	1.72 – 2.25	2 / 4	[2000 1900 1800] / [4000 3800 3600]	–	2 – 1.8 / 2 – 1.8	1 2 4 8 16 32 64 128
ADQ1600	1.4 – 1.8	1.6	–	–	1.6	1 2 4 8 16 32 64 128
SDR14	1.4 – 1.8	0.8	–	–	1.6	1 2 4 8 16 32 64 128

**Table 4: Parameters**

1. Limited by VCO. Other parameters may put tighter requirements on the tuning range.
2. Available clock frequency range. ADCaptureLab settings using PLL divider. SetPLL()
3. ADCaptureLab settings using clock distribution divider. SetPLLFreqDivider().

### 8.2 Setting the external clock on ADQ412.

The external clock of ADQ412 can be set to any value according to the “EXT CLK” column of the **Table 4**<sup>1</sup>. The combination with sample skip result in a set of available sampling frequencies, see **Table 5**, **Table 6** and **Figure 7**.

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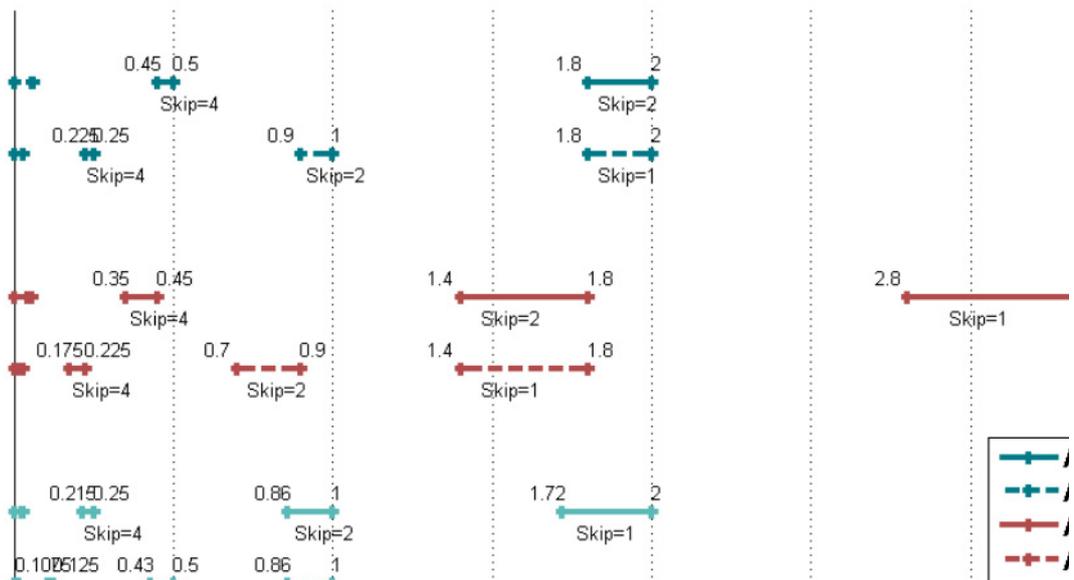
1. Correct function is not guaranteed outside these ranges.

SAMPLE SKIP	ADQ412-1G				ADQ412-3G				ADQ412-4G			
1	860	900	950	1000	1400	1500	1600	1700	1800	1800	1900	2000
2	430	450	475	500	700	750	800	850	900	900	950	1000
4	215	225	238	250	350	375	400	425	450	450	475	500
8	108	113	119	125	175	188	200	213	225	225	238	250
16	54	56	59	63	88	94	100	106	113	113	119	125
32	27	28	30	31	44	47	50	53	56	56	59	63
64	13	14	15	16	22	23	25	27	28	28	30	31
128	6.7	7.0	7.4	7.8	11	12	13	13	14	14	15	16

**Table 5: Sample skip clock frequencies in 4 channels mode**

SAMPLE SKIP	ADQ412-1G				ADQ412-3G				ADQ412-4G			
1	1720	1800	1900	2000	2800	3000	3200	3400	3600	3600	3800	4000
2	860	900	950	1000	1400	1500	1600	1700	1800	1800	1900	2000
4	430	450	475	500	700	750	800	850	900	900	950	1000
8	215	225	238	250	350	375	400	425	450	450	475	500
16	108	113	119	125	175	188	200	213	225	225	238	250
32	54	56	59	63	88	94	100	106	113	113	119	125
64	27	28	30	31	44	47	50	53	56	56	59	63
128	13	14	15	16	22	23	25	27	28	28	30	31

**Table 6: Sample skip clock frequencies in 2 channels mode**



**Figure 7: Clock frequencies for ADQ412 versions in 2 and 4 channels mode and sample skip.**

### 8.3 Setting the internal clock on ADQ412

The internal clock frequency can be set according to [Table 4](#)<sup>1</sup>. These settings are accessed via ADCaptureLab or the ADQ API command SetPLL(). The combination with sample skip result in a set of available sampling frequencies, see [Table 5](#), [Table 6](#) and [Figure 7](#).

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1. Correct function is not guaranteed outside these ranges.

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### Teledyne SP Devices Corporate Headquarters

Teknikringen 6  
SE-583 30 Linköping  
Sweden

Phone: +46 (0)13 465 0600

Fax: +46 (0)13 991 3044

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