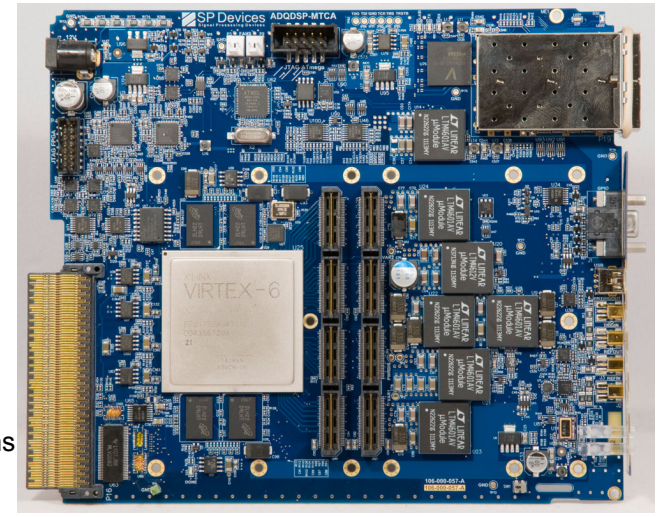
ADQDSP-MTCA is a digital signal processing board for signal recording and real time signal processing. Powered with a Virtex 6 LX240T FPGA and 1GByte data RAM, the ADQDSP-MTCA operates as a stand alone calculation board. The ADQDSP-MTCA is also prepared for analog front end boards connected through a daughter board connector with a capacity of eight 17 bits LVDS busses. A typical application is a high end digitizer.

Features

- Virtex 6 FPGA
- Data streaming mode
- 1GByte data memory
- Trigger IN/OUT
- Clock reference IN/OUT
- Daughter board connector
- Daughter board power supply
- Digitizer functions
- Data interface PCIe Gen1 x4
- FPGAs available for customized applications



Applications

- RADAR
- LIDAR
- Wireless communication
- Optical transmission
- High-speed data recording
- Test and measurement
- Ultrasonic ranging

Software support

- MATLAB
- C/C++

Ordering information

Table 1:

ORDERING INFORMATION	
See respectively digizer product	
RELATED PRODUCTS	
ADQ Development Kit	ADQ Dev Kit

Example: ADQ412-3G-MTCA

Introduction

The ADQDSP-MTCA is a digital signal processing board, tailored for digitizer functions and real time signal processing. The ADQDSP-MTCA has a high capacity connector for connecting analog front end boards (AFE). The AFE connector can (for example) interface up to 8 different 16 bit high speed ADCs or DACs.

The FPGA is a Virtex 6 LX240T. Parts of the FPGA are available for customized real time applications through the ADQ Development Kit. Using the ADQ Development Kit, the ADQDSP-MTCA board also operates as without an AFE as a real time computational board.

The ADQDSP-MTCA provides host connection through various interfaces.

ADQ Development Kit

SP Devices' ADQ Development Kit is an optional software tool that rapidly enhances the customization process of your next DSP application for the ADQDSP-MTCA onboard FPGA. More details about this product can be found in the product brief for the ADQ Development Kit.

1 Technical data[1]

Table 2:

KEY PARAMETERS	
Daughter board interface	136 Gbit/s
Daughter board width	136 bits
Data memory	8 Gbit
Memory bandwidth	92 Gbit/s
Host computer interface	400 MByte/s sustained data rate over x4 cPCIe/PXIe
Host computer interface	400 MByte/s sustained data rate
Trigger	Software / External / Edge
Number of GPIOs	5
Front panel connectors	MMCX / Micro-D Plug 9 way
Clock reference	Internal / External

Table 3:

INTERNAL CLOCK REFERENCE	
Clock references source	10 MHz external Internal TCXO

Table 4:

EXTERNAL CLOCK REFERENCE		
Frequency (min – max)	10 – 250	MHz
Signal level (min – max)	0.8 – 3.3	V_{PP}
Impedance AC	50	Ω
Duty cycle	50% ± 5%	

Table 5:

CLOCK REFERENCE OUTPUT		
Frequency (min – max)	10	MHz
Signal level	3.3	V_{PP}
Impedance AC	50	Ω
Duty cycle	50% ± 5%	

Table 6:

MEMORY	
Data memory	1GByte
Pre-trigger buffer	Up to batch size
Trigger hold off	2^{34} samples
Multi record batch size	Up to memory size
Multi record max PRF	1 MHz

Table 7:

EXTERNAL TRIGGER INPUT		
Input impedance DC	50	Ω
Input range (min – max)	–2.5 – +3.3	V
Threshold rising edge	0.5	V
Time resolution	250	ps

Table 8:

TRIGGER OUTPUT		
Output impedance	30	Ω
Output (low – high)	0.1 – 3.2	V

Table 9:

GPIO		
Number of GPIO	5	
Output imp. GPIO-pin	30	Ω
Output (low – high)	0.1 – 3.2	V
Input impedance	10	kΩ
Input (low – high)	1 – 2.3	V

Table 10:

POWER SUPPLY		
Supply voltage	12	V
Power consumption[1]	20	W

1. Not including any daughter board.

Table 11:

ENVIRONMENTAL / MECHANICAL		
Operating temperature	0 – 45	°C
Storage temperature	–20 – 70	°C
Relative humidity, non-condensing	5% – 95%	
Board size	Double width	
Board size	Mid size	

Table 12:

OPERATING SYSTEM	
Windows XP	SP 2 and higher
Windows Vista	All versions
Windows7	32b and 64b
Linux	Check for availability

Table 13:

APPLICATION SOFTWARE	
ADCaptureLab	Data capture and analysis
MATLAB	Data capture interface
C/C++	Data capture interface

1. All values are typical unless otherwise noted.

2 Architecture

2.1 Overview

The ADQDSP-MTCA performs the digital back end of a digitizer. COmbined with a front end card through the Daughter board connector, a digitizer is formed. The ADQDSP-MTCA controls the data acquisition, data storage and host connection.

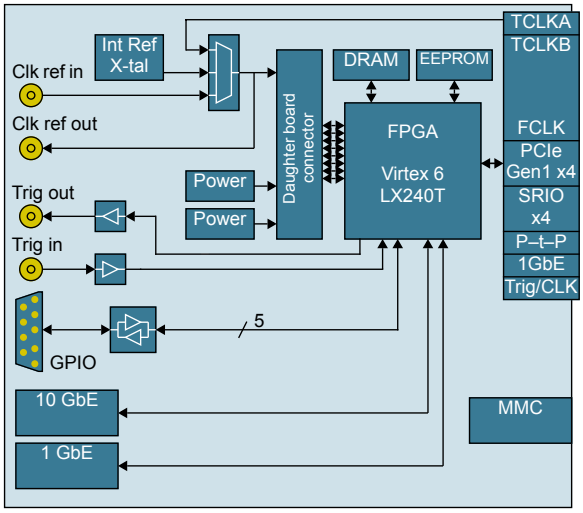


Figure 1: Block diagram

2.2 FPGA

The data outputs of the daughter board connector are connected to a Xilinx XC6VLX240T FPGA which is open for user applications through the ADQ Development Kit.

2.3 Memory

There is 1GByte data batch memory. The data batch length for each recording is set to any value within this range. For more information about memory handling, see **Section 3.1**.

2.4 Clock

The ADQDSP-MTCA provides several clock references for the daughter board.

- 10 MHz TCXO.
- External MMCX connector for an external clock reference.
- Back plane reference clock TCLKA, TCLKB.

More on clocking in **Section 2.5.1**.

2.5 Host Interface

The ADQDSP-MTCA is connected to the host through a Compact PCI Express interface. This interface handles data transfer and digitizer operations control.

The control of the board, surveillance and firmware upgrade is done via the MMC.

2.5.1 Clock signals

Different ADCs require different type of clocks. Therefore the PLL is placed on the daughter board. There are several connections between the boards. This is a typical solution. Not all daughter boards follow this system.

- A set of references are available from the ADQDSP-MTCA board. (External, internal and backplane clock)
- An external direct clock is on the daughter board.
- The ADC clock is generated in the PLL.
- The ADC data clock is routed to clock pins on the FPGA to clock data receivers.
- Two global clock pins in the FPGA are connected directly to the PLL for synchronized operations.

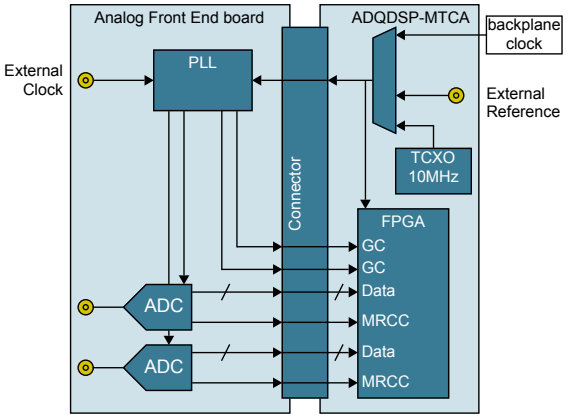


Figure 2: Clock of daughter board. Typical digitizer solution.

2.6 Hardware Triggers

2.6.1 Trigger Input

The trigger input is DC coupled with 50 ohm termination. The trigger threshold is fixed at 0.5 V. The contact type is MMCX.

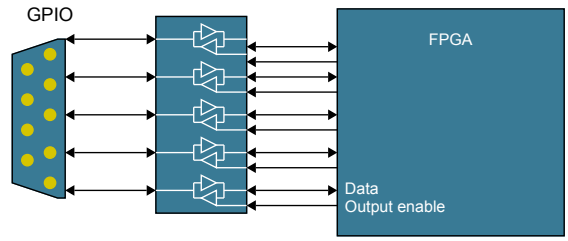
2.6.2 Trigger output

The trigger output is a high current short circuit protected digital output signal. The trigger output can be used for triggering several ADQDSP-MTCA boards through a single software command. The contact type is MMCX.

2.7 GPIO

The ADQDSP-MTCA is equipped with 5 bidirectional GPIOs. The GPIOs are controlled from software, but can also be accessed from the ADQ Development Kit.

The connector is Micro D plug 9 way. A suitable socket with lead is for example MOLEX 83421-9044.



#	Function
1	GPIO
2	GPIO
3	GPIO
4	GPIO
5	GPIO
6	GND
7	GND
8	GND
9	GND

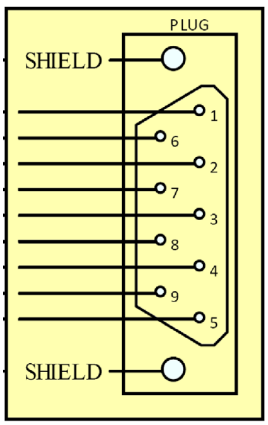


Figure 3: GPIO block diagram.

3 Digitizer functions

The ADQDSP-MTCA has a set of built in digitizer functions

3.1 Trigger

3.1.1 Overview

There are several trigger options

- Software trigger
- Level trigger rising/falling edge on different channel combinations
- External trigger
- Daughter board dedicated trigger

When armed, the system is waiting for the selected trigger event. At the trigger event, a data batch of selected length is recorded in the batch memory. A pre-trigger buffer is available. The length of the pre-trigger buffer is fully controllable[1]. The pre-trigger buffer is a part of the total batch length.

The trigger hold-off is up to 2^{34} samples and is set in steps of 2 samples.

3.1.2 Software trigger

Data capture is triggered by a software command. This is suitable for measurements on continuous waves.

3.1.3 Level trigger

Data capture is triggered by an event on the input data. This is useful for capturing pulses. The level trigger combined with the pre-trigger or trigger hold-off setting can capture any pulse shape.

3.1.4 External trigger

Data capture is triggered by positive edge on the trigger input connector. This is intended for synchronizing the signal source with the ADQDSP-MTCA. It can also be used for synchronizing several ADQDSP-MTCA.

3.1.5 Daughter board trigger

There is a dedicated differential pair in the daughter board connector for a specialized trigger on the daughter board.

1. There is a fixed amount of delay between the trigger and data depending on the length of the wires and the internal signal paths. This delay will change for a custom application using the ADQ Development Kit

3.1.6 Multi record

The ADQDSP-MTCA can be set up in a multi record mode. At each trigger, a record of data is recorded in the memory. The length of each record and number of records is user defined. Multi record works together with pre-trigger buffer and trigger hold off.

3.1.7 Time stamp

A 64 bits time counter, which runs on the sampling frequency, enables time stamp for each event. At each trigger event, the counter value is read and stored together with the data record.

The time counter starts at power up and may directly be used for relative time measurement. The counter can be reset by software. The counter can also be synchronized to an external start pulse. The external start pulse can operate in two modes; single start signal or repeated restart of the time counter. In the repeated restart mode, the counter is divided into a 42 bits time counter and a 22 bits start pulse counter.

The start pulse is connected to GPIO pin #2.

4 Communication interfaces

There are several options for communicating with the ADQDSP-MTCA.

Standard interfaces:

- PCIe Gen1 x4

Avalable through ADQ Development Kit

- 1GbE through backplane
- 1GbE in front panel
- 10GbE in front panel
- Point-to-point LVDS
- Trigger/Clock/Interlock
- SRIO x4

5 Software tools

5.1 ADCaptureLab

The ADQDSP-MTCA is supplied with the ADCaptureLab software that provides quick and easy control of the digitizer. The tool also offers both time domain and frequency domain analysis, see **Figure 4**. Data can be saved in different file formats for off-line analysis. Comparison of results is easily done by importing data from file and analyze it in ADCaptureLab.

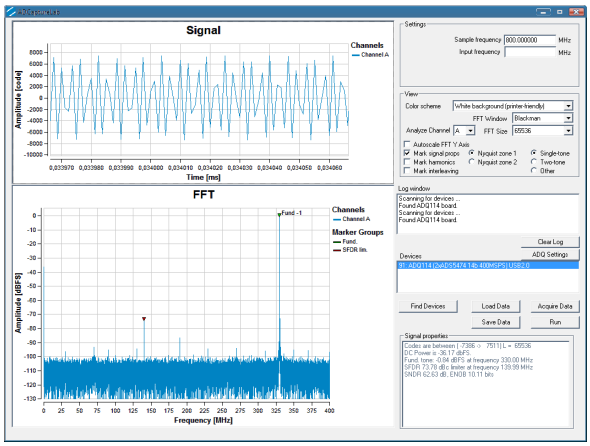


Figure 4: ADCaptureLab (Typical)

5.2 Software development kit (SDK)

The ADQDSP-MTCA digitizer system is easily integrated into your own application by using the included Software development kit. The SDK includes programming examples and reference projects for C/C++ and MATLAB.