ADQTDU

ADQTDU is a trigger and clock distribution unit for ADQ series of digitizer. The ADQTDU is available in several variants for different types of electrical signaling. The ADQTDU is also available in several form factors for integration different types of systems.

Introduction

The ADQTDU is a fan out buffer with 1 input and 6 outputs. The unit is used for trigger and clock distribution. See **Figure 1** for block diagram.

The ADQTDU is available with several options for logic levels, form factor, and control possibilities.

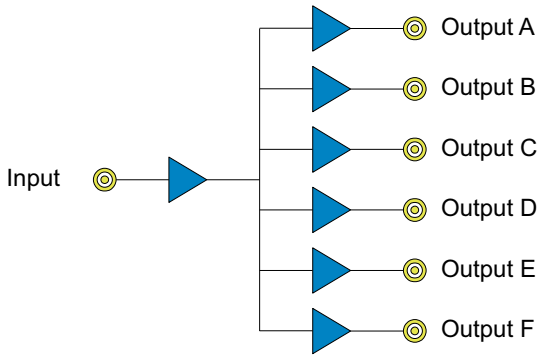

Figure 1: Block diagram of ADQTDU

TECHNICAL DATA[1]		
Number of inputs	1	
Number of outputs	6	
Power supply	12	V
Power consumption	2	W
Box size	103 x 166 x 31 mm^3	
Card size cPCIe/PXIe	1 slot 3U	
Connector	SMA	

1. ALL VALUES ARE TYPICAL UNLESS OTHERWISE NOTED.

Applications

The LVPECL configuration is ideal for driving clock or clock reference for several ADQ series digitizers.

The LVCMOS configuration is ideal for distributing the trigger to several ADQ series of digitizers.

Ordering information

ORDERING INFORMATION	
ADQTDU	ADQTDU
AVAILABLE OPTIONS	
CMOS	–C
LVPECL	–P
AC LVPECL	–AC
Control function (TBC)[1]	–CTRL
Stand alone box	–USB
cPCIe/PXIe	–PXIe

1. Contact SP Devices' sales representative for information on control option.

Example: ADQTDU–P–PXIe

CMOS options

The input is available as logic compatible comparator input and may be driven by TTL, CMOS, etc. The input is 50 Ohms terminated to ground to avoid reflections in cables. Due to the termination to ground, the threshold level is set to the level 0.7 V.

The output are short circuit protected CMOS compatibel drivers.

CMOS[1]			
Vth	Input threshold	0.7	V
Rin	Input impedance	50	Ohm
ViH	Input level High (min)	1.1	V
ViL	Input level Low (max)	0.3	V
VoH	Output level High (min)	2.5	V
VoL	Output level Low (max)	0.5	V
Rout	Output impedance	35	Ohms
	Output slew rate	5	V/ns
	Channel–channel skew	50	ps
	Propagation delay	2	ns
	Max frequency	200	MHz
	Additive jitter	250	fs

1. All values are typical unless otherwise noted.

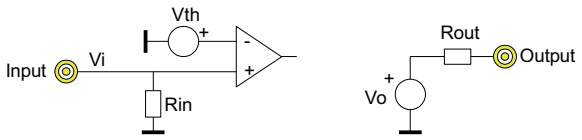

Figure 1: Equivalent circuit diagrams CMOS

Order code: –C

LVPECL option

The ADQTDU also available as single ended LVPECL.

Table 1:

DC COUPLED LVPECL[1]			
Vref	Reference voltage	1.3	V
Rin	Input impedance	50	Ohm
Vi	Input signal	0.5	Vpp
Vith	Input signal threshold	2	V
Vo	Output signal	0.6	Vpp
	Channel–channel skew	30	ps
	Propagation delay	220	ps
	Max frequency	2	GHz
	Additive jitter	75	fs

1. All values are typical unless otherwise noted.

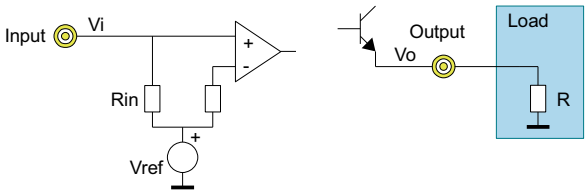

Figure 2: Equivalent circuit diagrams LVPECL

Order code: –P

AC coupled option

The LVPECL version is available for AC coupled systems. This is intended for clock distribution, where the signal is periodic.

The input is AC coupled an AC terminated 50 Ohms. Lower cut of frequency is 10 kHz.

The output has load resistors and is intended to drive AC coupled inputs.

Table 2:

AC COUPLED LVPECL[1]			
RDC	Input impedance DC	10k	Ohm
Rin	Input impedance AC	50	Ohm
Vi	Input signal	0.5	Vpp
Vo	Output level High (min)	1.9	V
VoL	Output level Low (max)	1.3	V
Rout	Built in load impedance	180	Ohm
	Channel–channel skew	30	ps
	Propagation delay	220	ps
	Max frequency	2	GHz
	Additive jitter	75	fs

1. All values are typical unless otherwise noted.

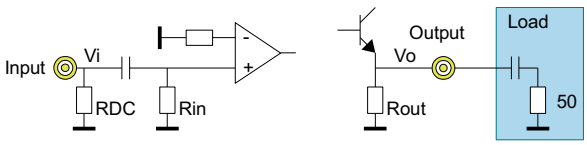

Figure 3: Equivalent circuit diagrams AC LCVPECL

Order code: –AC

Form factor option

The ADQTDU is available in a stand alone box. The box is supplied by an external 12 V power adapter.

Avalability TBC.

Figure 4: Typical box version

Order code: –USB

The ADQTDU is available in cPCIe/PXIe form factor. It uses only power supply from the chassis.

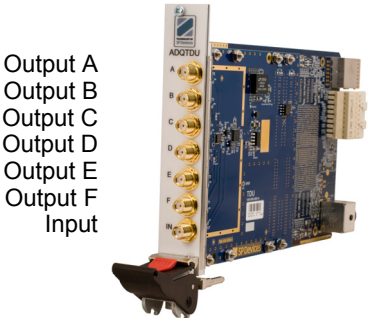

Figure 5: ADQTDU–PXIe form factor

Order code: –PXIe

Controlling the output (TBC)[1]

The CMOS version is available with a controller interface to turn off the trigger signal. Through an API command, the outputs may be set at high or low. On command, the signal is turned on again. This enable signal may also come from an external input. The enable signal is available at an output for a chain connection of units.

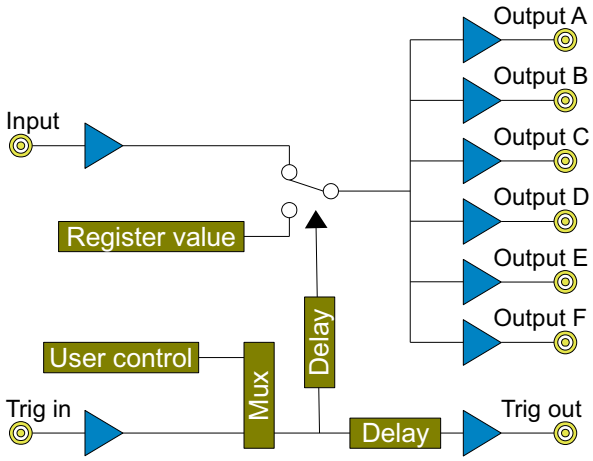

Figure 6: Block diagram of ADQTDU

This function is intended for systems where the trigger signal source is free running and may not be stopped. The sequence of operation is then

1. Set the trigger signal to low
2. Set up all digitizers
3. Send trigger arm command to each of them
4. Turn on the trigger signal

The digitizers will then start simultaneously on the same trigger.

By setting the delay lines, several ADQTDU can be controlled in phase by the same signal, **Figure 7**.

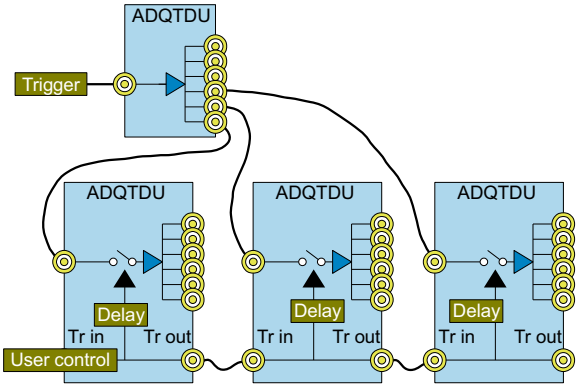

Figure 7: Chain of control for ADQTDU

Table 3:

CONTROL OPTION[1]			
P	Power consumption	20	W

1. All values are typical unless otherwise noted.

Order code: –CTRL

1. Contact SP Devices' sales representative for information about the control option.

Important Information

Teledyne Signal Processing Devices Sweden AB (Teledyne SP Devices) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to Teledyne SP Devices' general terms and conditions supplied at the time of order acknowledgment.

Teledyne SP Devices warrants that each product will be free of defects in materials and workmanship, and conform to specifications set forth in published data sheets, for a period of one (1) year. The warranty commences on the date the product is shipped by Teledyne SP Devices. Teledyne SP Devices' sole liability and responsibility under this warranty is to repair or replace any product which is returned to it by Buyer and which Teledyne SP Devices determines does not conform to the warranty. Product returned to Teledyne SP Devices for warranty service will be shipped to Teledyne SP Devices at Buyer's expense and will be returned to Buyer at Teledyne SP Devices' expense. Teledyne SP Devices will have no obligation under this warranty for any products which (i) has been improperly installed; (ii) has been used other than as recommended in Teledyne SP Devices' installation or operation instructions or specifications; or (iii) has been repaired, altered or modified by entities other than Teledyne SP Devices. The warranty of replacement products shall terminate with the warranty of the product. Buyer shall not return any products for any reason without the prior written authorization of Teledyne SP Devices.

In no event shall Teledyne SP Devices be liable for any damages arising out of or related to this document or the information contained in it.

TELEDYNE SP DEVICES' EXPRESS WARRANTY TO BUYER CONSTITUTES TELEDYNE SP DEVICES' SOLE LIABILITY AND THE BUYER'S SOLE REMEDY WITH RESPECT TO THE PRODUCTS AND IS IN LIEU OF ALL OTHER WARRANTIES, LIABILITIES AND REMEDIES. EXCEPT AS THUS PROVIDED, TELEDYNE SP DEVICES DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING ANY WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT.

TELEDYNE SP DEVICES DOES NOT INDEMNIFY, NOR HOLD THE BUYER HARMLESS, AGAINST ANY LIABILITIES, LOSSES, DAMAGES AND EXPENSES (INCLUDING ATTORNEY'S FEES) RELATING TO ANY CLAIMS WHATSOEVER. IN NO EVENT SHALL TELEDYNE SP DEVICES BE LIABLE FOR SPECIAL, INCIDENTAL OR CONSEQUENTIAL DAMAGES, INCLUDING LOST PROFIT, LOST DATA AND THE LIKE, DUE TO ANY CAUSE WHATSOEVER. NO SUIT OR ACTION SHALL BE BROUGHT AGAINST TELEDYNE SP DEVICES MORE THAN ONE YEAR AFTER THE RELATED CAUSE OF ACTION HAS ACCRUED. IN NO EVENT SHALL THE ACCRUED TOTAL LIABILITY OF TELEDYNE SP DEVICES FROM ANY LAWSUIT, CLAIM, WARRANTY OR INDEMNITY EXCEED THE AGGREGATE SUM PAID TO SP BY BUYER UNDER THE ORDER THAT GIVES RISE TO SUCH LAWSUIT, CLAIM, WARRANTY OR INDEMNITY.

Worldwide Sales and Technical Support

www.spdevices.com

Teledyne SP Devices Corporate Headquarters

Teknikringen 6
SE-583 30 Linköping
Sweden

Phone: +46 (0)13 465 0600
Fax: +46 (0)13 991 3044
Email: info@spdevices.com