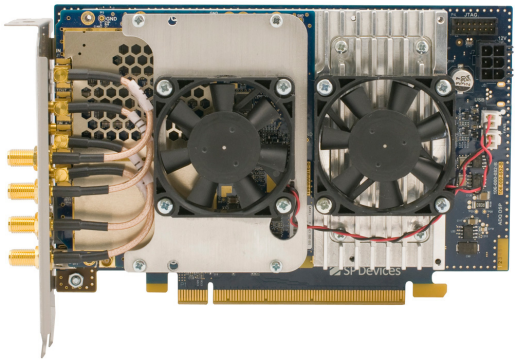
ADQ1600TD

ADQ1600TD is a unique member of the ADQ V6 Digitizer family. Based on SP Devices' interleaving technologies ADX and DBS, ADQ1600TD gets true 14 bits performance at a sampling rate of 1.6 GSPS. This is an outstanding combination of high bandwidth and dynamic range, which enables demanding measurements such as sampling of very narrow pulses.



Introduction

The ADQ1600TD delivers 14 bits resolution at the sampling rate 1.6 GSPS. The high sample rate combined with the unique dynamic range is tailored for wide band measurements. The software controllable input bias function makes ADQ1600TD an ideal tool for capturing fast pulses.

The ADQ1600TD offers an easy-to-use API that allows easy integration into any application. The digitizer connects to the host via a SuperSpeed USB cable for stand-alone operation. It is also available in cPCIe / PXIe / Micro-TCA.4 form factor for modular instrumentation and in PCIe form factor for compact integration in a stationary PC.

The ADQ1600TD is equipped with a powerful Xilinx V6 LX240T FPGA which is partly available for customized real-time applications.

ADQ1600 Development Kit

SP Devices' ADQ1600 Development Kit is an optional tool for integrating custom real-time signal processing in the FPGA. The custom firmware is easily integrated into the digitizer's standard functions to enhance the capabilities of demanding signal analysis. More details about this product can be found in the datasheet for the ADQ Development Kit.

Ordering information

ORDERING INFORMATION	
Order code	ADQ1600TD
AVAILABLE OPTIONS	
USB3 interface	–USB
cPCIe / PXIe interface	–PXIE
PCIe interface	–PCIE
Micro-TCA interface	–MTCA
RELATED PRODUCTS	
ADQ1600 Development Kit	

Features

- 1 analog input channel
- 1.6 GSPS sampling rate
- 14 bits resolution
- 680 MHz analog bandwidth (–3dB)
- Internal and external clock reference
- Internal and external clock source
- Clock reference output
- 2 external trigger inputs
- Trigger output
- Internal trigger pulse generator
- Time stamp
- Waveform averaging
- Variable bias
- Multi-record >1 MHz PRF
- 512 Msamples data memory
- Data interface USB 3.0 / cPCIe / PXIe / PCIe / Micro-TCA
- 3.5 GBytes/s data transfer rate on Gen2 by 8 lanes
- FPGA open for real-time custom applications

Applications

- Time-of-flight
- Physics experiments
- LIDAR
- Wireless communication
- Optical transmission
- High-speed data recording
- Test and measurement
- Ultrasonic ranging

1 Technical data[1]

Table 1:

ANALOG INPUT		
Number of channels	1	
Digitizer Resolution	14	bits
Sample rate	1600	MSPS
SFDR @ 30 MHz	68	dB
SNR @ 30 MHz	68	dB
Impedance AC	50	Ω
Input voltage range	2.2	V_{pp}
Analog bandwidth (–3dB)	35 Hz – 680 MHz	
Bias setting range	Full signal range	
Bias setting steps	31 levels	
Connector	SMA	

Table 2:

EXTERNAL CLOCK SOURCE		
Frequency	FS	MHz
Signal level (min – max)	0 – 10	dBm
	0.64 – 2	Vpp
Impedance AC	50	Ω
Duty cycle	50%	
Connector	SMA	

Table 3:

CLOCK REFERENCE INPUT		
Internal clock reference		
Frequency	10	MHz
Accuracy	± 5 ± 0.5/y	ppm
External clock reference		
Frequency (min – max)	1 – 250	MHz
Signal level (min – max)	0.8 – 3.3	V_{PP}
Impedance AC	50	Ω
Duty cycle	50% ± 5%	
Connector PCIe / PXIe	MCX	
PXIe clock reference[1]		
PXIe clock	100	MHz
PXIe sync[2]	10	MHz

1. Available on PXIe form factor only.
2. Jitter reduced by PXIe clock in digitizer.

Table 4:

CLOCK REFERENCE OUTPUT		
Frequency	Same as clock reference	
Signal level	3.3	V_{PP}
Impedance AC	50	Ω
Duty cycle	50% ± 5%	
Connector PCIe / PXIe	MCX	

Table 5:

EXTERNAL TRIGGER INPUT 1		
Input impedance DC	50	Ω
Input range (min – max)	–0.4 to 2.4	V
Threshold rising/falling edge	500	mV
Sensitivity	200	mV
Jitter	25	ps
Resolution	1/FS	s
Connector	MCX	

Table 6:

EXTERNAL TRIGGER INPUT 2		
Input impedance DC	50	Ω
Input range (min – max)	–0.5 to 3.5	V
Threshold rising/falling edge tuning range	0 to 3300	mV
Sensitivity	200	mV
Jitter	25	ps
Resolution	1/FS	s
Connector	SMA	

Table 7:

TRIGGER OUTPUTS[1]		
Output impedance	30	Ω
Output (low – high)	0.1 – 3.2	V
Connector Trigger 1	MCX	
Connector Trigger 2	SMA	

1. There are 2 different trigger outputs, but there is only one core for generating trigger signals.

Table 8:

GPIO		
Number of GPIO	5	
Output impedance pin #5	33	Ω
Output impedance pin #1–4	100	Ω
Output (low – high)[1]	0.1 – 3.2	V
Input impedance	10	kΩ
Input (low – high)	1 – 2.3	V
Connector	Micro DSUB 9 way	

1. Unloaded condition.

1. All values are typical unless otherwise noted.

Table 9:

POWER SUPPLY		
Supply Voltage	12	V
Power[1]	42	W
Connector USB	Included power supply	
Connector PCIe	6-pin ATX power	
Connector cPCIe/PXIe	from slot	
Connector MTCA	from slot	

1. Measured with standard firmware in status waiting for trigger which represents a high activity. Power consumption is dependent of activity.

Table 10:

CERTIFICATION AND COMPLIANCE
CE

Table 11:

LED INDICATORS		
Power	Green	Power up
Ready	Yellow	Waiting for trigger
Status	Red	Flashing overheat

2 Architecture

2.1 Block diagram

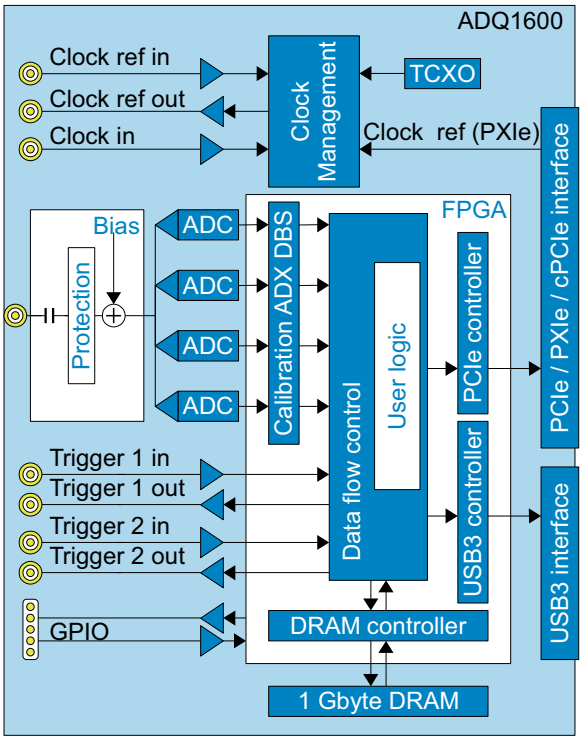


Figure 1: Block diagram.

A block diagram of the digitizer is shown in **Figure 1**. The main blocks are described below.

2.2 Analog front-end

The analog front-end contains AC-coupling, over-voltage protection, termination and step response control and variable bias.

2.3 Interleaving Technology ADX and DBS

The unique sample rate, 1600 MSPS with maintained 14 bits performance, is achieved by interleaving four ADCs. Typical interleaving artifacts are removed by SP Devices' proprietary interleaving technologies ADX and DBS, which run in the FPGA.

2.4 Digital data format

The ADQ1600TD is a 14-bit digitizer but the word length is extended to 16 bits (MSB aligned) internally to allow for performance improvement through digital calibration and interleaving correction. This word extension is also beneficial for situations where custom firmware is added through use of the ADQ1600 Development Kit.

3 Pulse capture support

The analog input and digital signal processing is optimized for capture of unipolar pulses in several ways, see **Figure 2**.

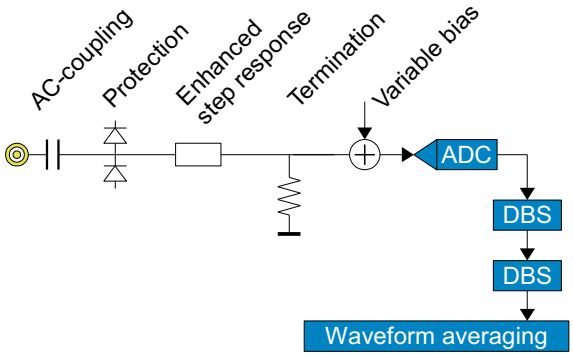


Figure 2: Analog front-end and signal processing for pulse measurement.

AC–coupling: The input is AC-coupled to achieve maximum dynamic range.

Over-voltage protection: The over-voltage protection makes the digitizer robust to unintended over-voltage from fast amplifiers.

Enhanced step response: The effect of AC-coupling on the signal baseline is suppressed by SP Devices' technology for enhanced step response, **Figure 3**.

Variable bias: The variable bias enable the use of the entire dynamic range for sampling unipolar pulses. This is achieved by adjusting the analog baseline to a level near the end of the analog signal range, **Figure 4**. The bias is set in 31 steps and is user controlled via software.

DBS: The digital baseline stabilizer, DBS, sets the baseline to a target level in the digital domain. DBS suppresses interleaving effects on the baseline and also guarantees temperature stability.

ADX: The interleaving technology ADX operates in the background to suppress interleaving effects and enable a high sample rate

WFA: The signal processing core of ADQ1600TD also provides real-time waveform averaging as a powerful tool for data reduction and signal quality enhancement during pulse capture.

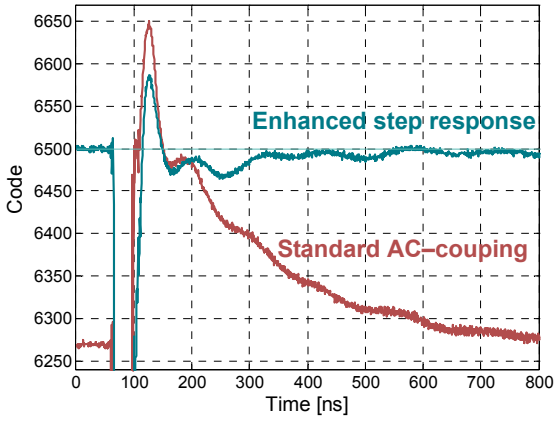


Figure 3: Technology for enhanced step response.

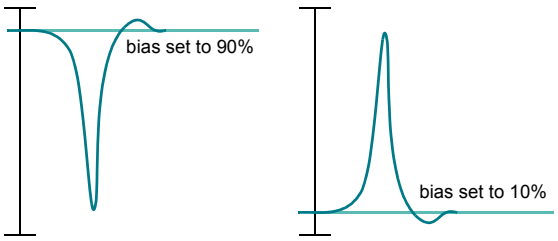
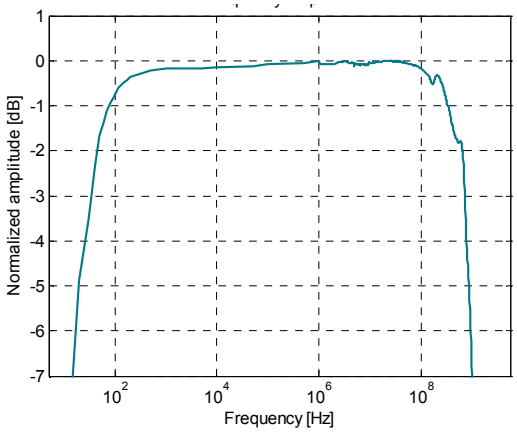


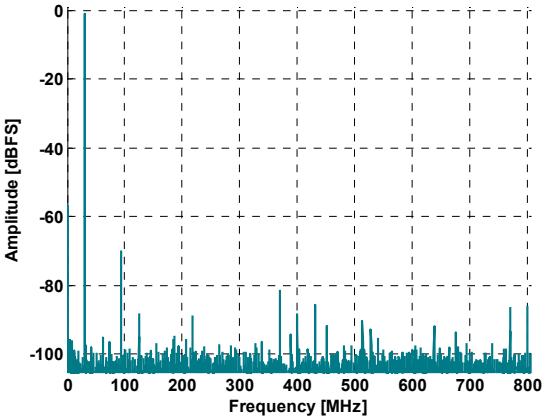
Figure 4: Variable bias, example of settings

4 Dynamic performance[1]



Signal bandwidth (–3dB)	35 Hz – 680 MHz
1 dB flatness	80 Hz – 420 MHz

Figure 5: Input signal frequency response.



Signal frequency	30 MHz
Sampling rate	1.6 GSPS
HD2	–93 dBc
HD3	–68 dBc
SNR	68 dB
ENOB	10.5 bits

Figure 6: Typical spectrum at 30 MHz.

1. All values are typical unless otherwise noted.

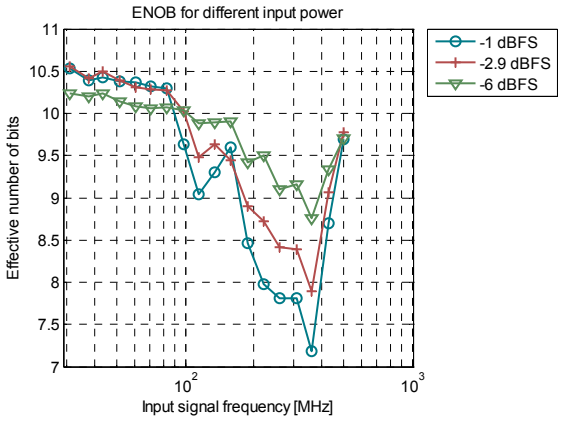


Figure 7: ENOB for different input power levels versus input signal frequency.

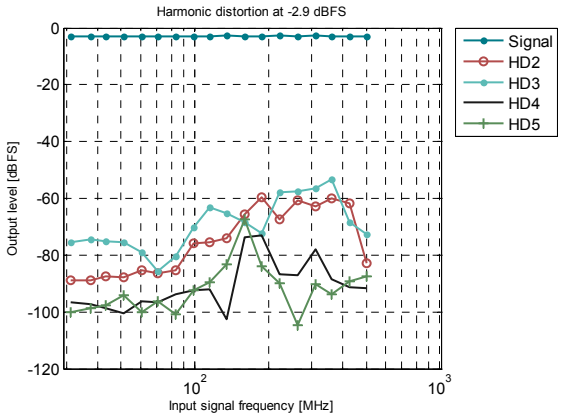


Figure 8: Harmonic distortion level for input signal power –2.9 dBFS versus input signal frequency.

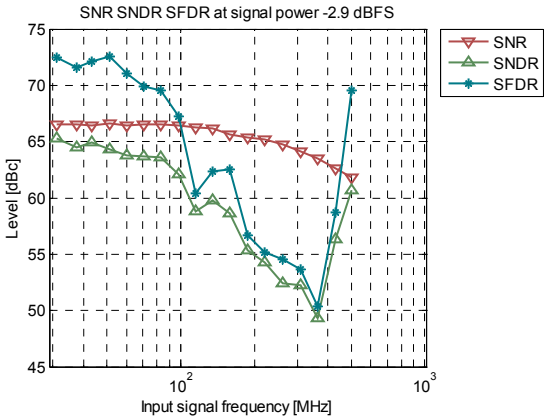


Figure 9: SNR, SFDR and SNDR for input signal power –2.9 dBFS versus input signal frequency.

5 Functional overview

5.1 Data recording

There are several methods for data recording to serve different use cases;

- Multi-record recording in on-board DRAM for very long records.
- Continuous multi-record via on-board DRAM for acquisition of long records during long measurement time.
- Continuous streaming of data to the host PC for real-time analysis of data[1].

To support data recording, there is on-board DRAM of 1 GBytes. The interface to the host PC enables up to 3.5 GBytes/s over a Gen2 x8 PCIe interface.

5.2 Signal processing

There is support for real-time signal processing on the digitizer;

- Real-time waveform averaging.
- Level trigger for event detection.
- Gain and offset calibration.
- Sample skip for data rate reduction.
- Custom real-time signal processing can be implemented using the ADQ1600 Development Kit.

5.3 Trigger

There are several trigger modes;

- External trigger for synchronization
- Level trigger for data driven acquisition
- Software trigger for user's control
- Internal trigger for automatic sequencing

There is also a trigger output for triggering external equipment. The trigger timing is controlled by pre-trigger buffer and trigger hold-off parameter settings.

5.4 Clock

There are several modes for clocking the digitizer;

- Internal clock for stand alone operation
- External clock for synchronization

1. If the host PC does not support full speed data transfer, data reduction in the FPGA is required. Sample skip and waveform averaging are included methods for this. Other data reduction can be achieved by implementing a custom algorithm using the ADQ1600 Development Kit.

- External clock reference for synchronization

There is also a clock reference output for clocking external equipment.

5.5 GPIO

There are 5 GPIO pins for real-time communication with external equipment. The GPIOs are controlled from software, but can also be accessed from the ADQ1600 Development Kit for integration in a real-time control system.

GPIO pin #2 may also be used for timestamp synchronization signal, for example a GPS 1 PPS.

The connector is Micro DSUB 9 way plug. A suitable socket with lead is for example MOLEX 83421-9044.

#	Function
1	GPIO pin #1
2	GPIO pin #2
3	GPIO pin #3
4	GPIO pin #4
5	GPIO pin #5
6	GND
7	GND
8	GND
9	GND

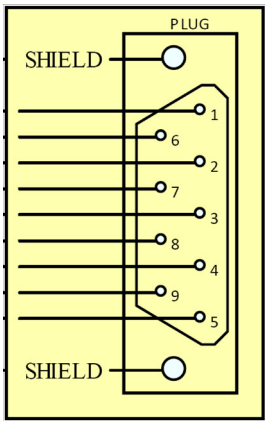


Figure 10: GPIO connector.

6 Absolute maximum ratings

Exposure to conditions exceeding these ratings may reduce lifetime or permanently damage the device.

The ADQ1600TD has a built-in fan to cool the device. The built-in temperature surveillance unit will protect the ADQ1600TD from overheating by temporarily shutting down parts of the device in such a situation.

The SMA connectors have an expected life time of 500 operations. For frequent connecting and disconnecting of cables, connector savers are recommended.

Table 12:

ABSOLUTE MAXIMUM RATINGS	MIN	MAX
Supply voltage (to GND)	–0.4 V	14 V
Trigger input 1 (to GND)	–3 V	3.7 V
Trigger input 2 (to GND)	–2.3 V	4.3 V
Clock ref (AC)		3.3 V_{PP}
GPIO input (to GND)[1]	–1 V	4.6 V
Ambient temperature (operation)	0 °C	45 °C
Analog inputs		
AC		10 V_{pp}
DC	–5 V	5 V

1. A voltage on a GPIO input higher than 3.3 V may change the output voltage on GPIOs which are set to outputs. This may damage external equipment.

7 Software tools

7.1 Operating systems

The software package includes drivers for the main operating systems.

Table 13:

OPERATING SYSTEM	
Windows XP	SP 2 and higher
Windows Vista	All versions
Windows 7	32 bit and 64 bit
Windows 8	32 bit and 64 bit
Linux[1]	Kernel 2 and 3, 32 and 64 bits

1. Contact SP Devices sales representative for information about distributions.

7.2 ADCaptureLab

The ADQ1600TD is supplied with the ADCaptureLab software that provides quick and easy control of the digitizer. The tool also offers both time domain and frequency domain analysis, see **Figure 11**. Data can be saved in different file formats for off-line analysis. With ADCaptureLab, the ADQ1600TD operate as a desktop oscilloscope.

Please note that ADCaptureLab is available for Windows only.

7.3 Software development kit (SDK)

The ADQ1600TD digitizer is easily integrated into the application by using the software development kit. The SDK is included with the ADQ1600TD.

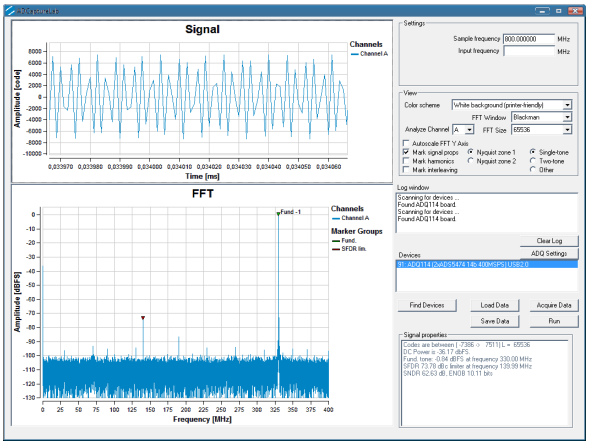


Figure 11: ADCaptureLab (Typical)

The SDK includes programming examples and reference projects for C/C++ and MATLAB. The ADQAPI user's guide in detail describes all functions. A set of examples and application notes simplify the integration process.

Using the SDK enables rapid custom processing of large amounts of data and real-time control of the digitizer.

Table 14:

APPLICATION SOFTWARE	
ADCaptureLab	Data capture and analysis
MATLAB	Data capture API, examples
C/C++	Data capture API, examples
Python	Limited example scripts
LabView[1]	Limited support

1. Contact SP Devices sales representative for guidance.

7.4 Data interface options

The ADQ1600TD is available in several form factors to suit various integration situations. The form factor sets the communication interface to the host PC as well as the mechanical properties of the ADQ1600TD.

The SuperSpeed USB (USB 3.0) interface is intended for stand alone operation and integration into the sensor system rather than the host PC.

The cPCIe, PXIe and M-TCA.4 from factors are intended for integration into a rack for modular instrumentation or large scale acquisition.

The PCIe form factor is for integration into the host PC. The board is half length to enable compact solutions.

Also the PCI-Express based models are equipped with a USB2.0 interface. It is intended for restoring the system if a custom firmware has failed.

7.5 PCI Express interface

The PCI Express interface is intended for integration in a PC.

Table 15:

PCIe INTERFACE		
Data rate	Gen2	
Bus width electrical	8	lanes
Sustained data rate, 8 lanes[1]	3.5	GByte/s
Bus width mechanical[2]	16	lanes
Board height	2	slots
Board length (half length)	167	mm

1. This is depending on the capacity of the complete system including the selected PC.
2. The wide contact is required to support the weight of the board.

Figure 12: ADQ1600TD–PCIE front panel.

Order code: –PCIE

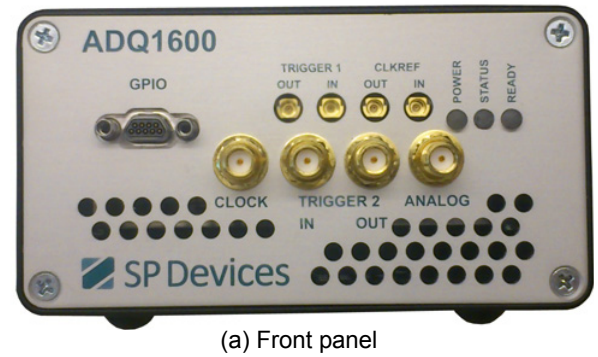
7.6 USB 3.0 interface

With the USB 3.0 interface, the digitizer is easily connected to any computer.[1, 2]

Table 16:

USB INTERFACE		
Standard	USB3	
Data rate sustained[1]	180	MB/s
Box size	53 x 106 x 166	mm3

1. This is depending on the capacity of the complete system including the selected PC.



(a) Front panel

(b) Rear panel

Figure 13: ADQ1600TD–USB panels

Order code: –USB

7.7 cPCIe / PXIe interface

The ADQ1600TD is available with cPCIe / PXIe interface.

Table 17:

cPCIe / PXIe INTERFACE		
Bus width	8	lanes
Bus peak capacity	16	Gbit/s
Sustained data rate[1]	3.5	GByte/s
PXIe card size	3U 2 slot 8TE	

1. This is depending on the capacity of the complete system including the selected PC.

Figure 14: ADQ1600TD–PXIE front panel.

Order code: –PXIE

1. USB 3.0 form factor is only supported under Windows 7 and Windows 8. Please contact an SP Devices sales representative for information about Linux support.
2. Note that only one digitizer at the time can be connected to a PC.

7.8 Micro-TCA interface

The ADQ1600TD is available with digital back-end and interfaces for Micro-TCA chassis, **Figure 15**.

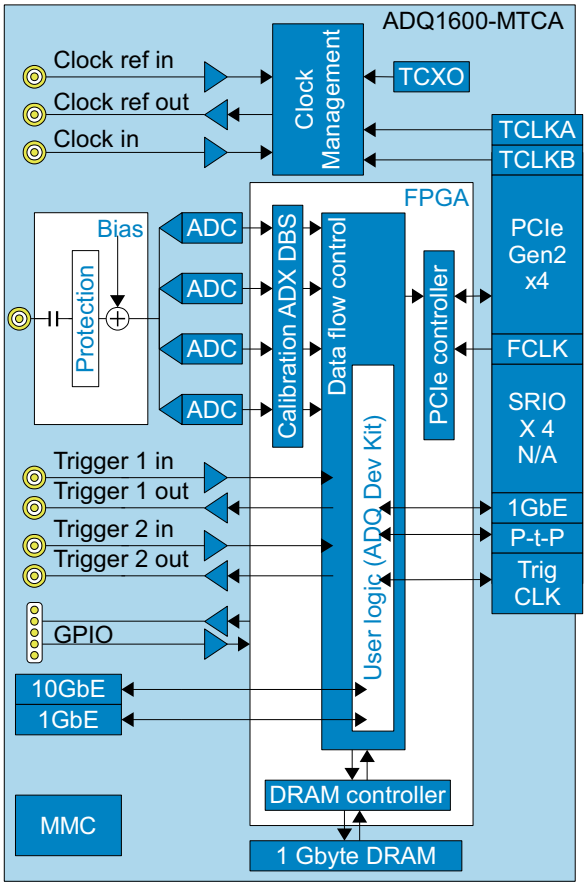


Figure 15: Block diagram of ADQ1600-MTCA.

Table 18:

MICRO-TCA BOARD SIZE	
Board width	Double width
Board height	Mid-size

Some of the pins in the backplane connector are used for the standard digitizer functions. Some are available for custom design using the ADQ1600 Development Kit for custom implementations only.

Table 19:

MICRO-TCA INTERFACE		
Signal	**Port**	**Status**
1GbE	0	ADQ1600TD Dev Kit
PCIe	4-7	Standard
Point-to-point	12-15	ADQ1600TD Dev Kit
Trigger, Data, Clocks	17-20	ADQ1600TD Dev Kit
TCLKA	Clk 1	Standard
TCLKB	Clk 2	Standard
FCLKA	Clk 3	Standard

Table 20:

FRONT PANEL ADDITIONAL INTERFACE		
Signal	**Connector[1]**	**Status**
1 GbE	SFP	ADQ1600TD Dev Kit
10 GbE	SFP+	ADQ1600TD Dev Kit

1. **SFP+ and SFP modules are not included.**

Figure 16: Typical Micro-TCA card

Order code: –MTCA

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