ADQ214

ADQ214 is a dual channel high speed digitizer. The ADQ214 has outstanding dynamic performance from a combination of high bandwidth and high dynamic range, which enables demanding measurements such as wide band data analysis and RF/IF sampling. Excellent spectral purity in combination with low noise makes ADQ214 ideal for noise measurements. ADQ214 features signal processing capacity for high speed pulse capture.

Introduction

The ADQ214 digitizer features dual channels, 14 bits resolution, 400 MSPS capture rate with 850 MHz analog input bandwidth, and 64 MSamples per channel memory buffer.

There are software selectable AC or DC coupled analog front ends available. The AC AFE is optimized for spectral purity over several nyquist bands, which makes it ideal for IF/RF sampling. The DC AFE is optimized for broadband applications such as base band signaling and high-speed data recording. Built in averaging and pre-biased front end option is ideal for pulse measurements

The ADQ214 offers an easy-to-use API that allows easy integration into any application. The card connects to the host via a high speed USB 2.0 cable. cPCIe / PXIe Gen 1 x4 interface is available as an option. The ADQ214 is equipped with two advanced Xilinx V5 series FPGAs that are available for customized real time applications.

ADQ214 Development Kit

SP Devices' ADQ214 Development Kit is an optional software tool that rapidly enhances the customization process of your next DSP application for the ADQ-series onboard FPGAs. More details can be found in the datasheet for the ADQ214 Development Kit.

Ordering information

ORDERING INFORMATION	
ADQ214 standard USB	ADQ214
OPTIONS	
cPCIe / PXIe	–PXIE
Positive bias	–PB
Negative bias	–NB
RELATED PRODUCTS	
ADQ214 Development Kit	ADQ214 Dev Kit

Features

- 2 channels
- AC/DC coupling
- 400 MSPS sampling rate
- 850 MHz analog bandwidth
- 14 bits resolution
- Internal and external clock
- External trigger
- Multi record >1 MHz PRF
- Time stamp per sample precision
- 64 MSamples data memory per channel
- Data interface USB 2.0 / cPCIe / PXIe
- Decimation filter and sample skip
- Waveform averaging
- Open FPGA for customized applications

Applications

- RADAR
- LIDAR
- Wireless communication
- Optical transmission
- High-speed data recording
- Test and measurement

Software support

- C/C++ API
- ADCaptureLab graphical tool
- MATLAB example
- LabView example (TBC)
- Phyton example

1 Technical data[1]

KEY PARAMETERS	
Number of channels	2
Digitizer Resolution	14 bits
Sampling rate	70 - 400 MSps
Data memory	64 MSamples/Channel
Trigger	Software / External / Edge
Number of GPIOs	5 + 1
Front panel connectors	SMA / Micro-D Plug 9 way
Clock	Internal / External / Ext ref

ANALOG INPUT AC		
ENOB @ 70 MHz	11	bits
SFDR @ 70 MHz	85	dB
Channel isolation @ 79 MHz	115	dB
Impedance DC	50	Ω
Bandwidth (–3 dB)	10 Hz–850 MHz	
Input voltage range	2.2	V_{PP}

ANALOG INPUT DC		
ENOB @ 70 MHz	8.5	bits
SFDR @ 70 MHz	67	dB
Impedance DC	50	Ω
Bandwidth (–3 dB)	350	MHz
Input voltage range	2.2	V_{PP}

INTERNAL CLOCK		
Accuracy	400	fs RMS
Internal sampling rate	800/n, n=2...11	MHz
Clock references source	10 MHz external Internal TCXO	

EXTERNAL CLOCK		
Frequency (min – max)	70 - 400	MHz
Signal level (min – max)	0.25 – 2	V_{PP}
Impedance AC	50	Ω
Duty cycle	50% ± 5%	

EXTERNAL REFERENCE		
Frequency	10	MHz
Signal level (min – max)	0.8 – 3.3	V_{PP}
Impedance AC	50	Ω

EXTERNAL TRIGGER INPUT/OUTPUT		
Input impedance DC	50	Ω
Input range (min – max)	–2.5 – +3.3	V
Threshold rising edge	0.5	V
Time resolution	625	ps
Output impedance	20	Ω
Output (low – high)	0.1 – 2	V

GPIO		
Output imp. GPIO-pin 5	30	Ω
Output imp. GPIO-pin 1–4	100	Ω
Output (low – high)	0.1 – 3.2	V
Input impedance	10	kΩ
Input (low – high)	1 – 2.3	V

MEMORY	
Data memory	64 MSamples/Channel
Pre-trigger buffer	Up to batch size
Trigger hold off	2^{33} samples
Multi record batch size	1 – entire memory
Multi record max PRF	1.6 MHz

HI-SPEED USB 2.0 INTERFACE		
Sustained data rate	25	MByte/s
Connector	Mini–B	

POWER SUPPLY		
Supply voltage	12	V
Power consumption	20	W

ENVIRONMENTAL / MECHANICAL		
Operating temperature	0 – 45	°C
Storage temperature	–20 – 70	°C
Relative humidity, non-condensing	5% – 95%	
Case size	103 x 166 x 31	mm^3

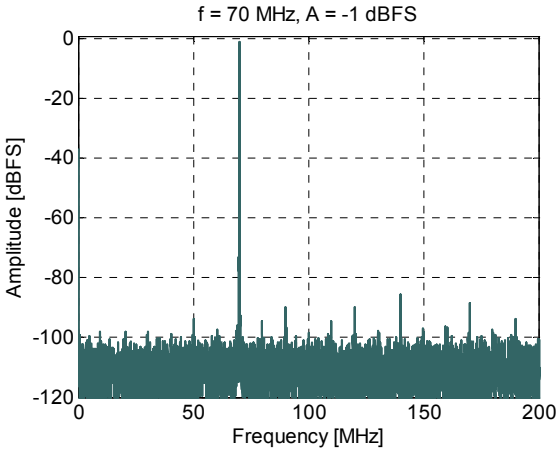
OPERATING SYSTEM	
Windows XP	SP 2 and higher
Windows Vista	
Windows 7	
Linux	

CERTIFICATION AND COMPLIANCE
CE, FCC Part 15 B

1. All values are typical unless otherwise noted.

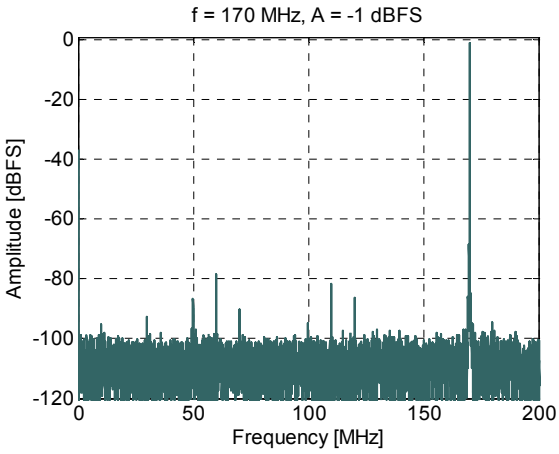
1 Analog front end

1.1 AC AFE



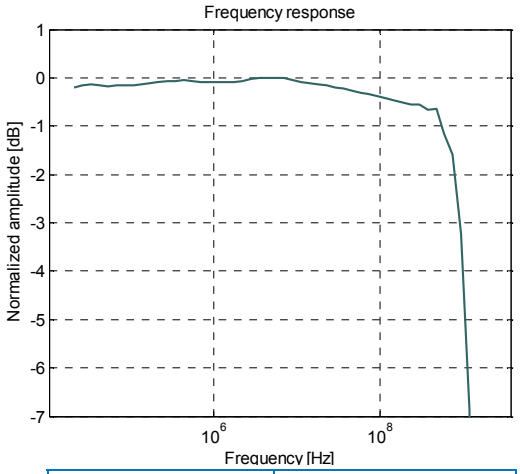
SFDR	85	dB
SNR	69	dB
ENOB	11	bits

Figure 1: AC AFE FFT of 70 MHz input signal.



SFDR	78	dB
SNR	67	dB
ENOB	10.8	bits

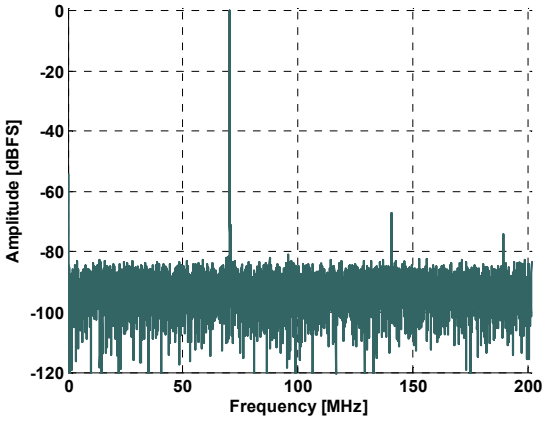
Figure 2: AC AFE FFT of 170 MHz input signal.



Full scale	2.2 V_{PP}
Bandwidth (–3 dB)	10 Hz – 850 MHz
1 dB flatness	20 Hz – 750 MHz

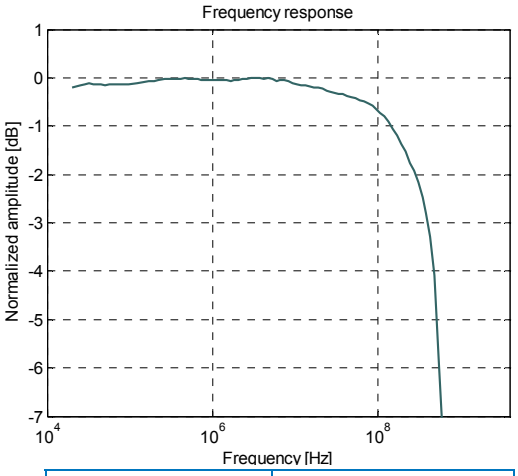
Figure 3: AC AFE frequency response.

1.2 DC AFE



SFDR	67	dB
SNR	54	dB
ENOB	8.5	bits

Figure 4: DC AFE FFT of 70 MHz input signal.



Full scale	2.2 V_{PP}
Bandwidth (–3 dB)	390 MHz
1 dB flatness	140 MHz

Figure 5: DC AFE frequency response.

1.3 Selecting analog front end.

The analog front end is selected with a software command. The setting is individual for the channels. Thus, one channel may use the AC AFE and one channel may use the DC AFE simultaneously.

1.4 Calibration

The default gain and offset setting for the AC AFE uses the intrinsic code mapping in the ADC. This is to reach optimal spectral purity.

The gain in the DC AFE is calibrated to match the gain in the AC AFE at 70 MHz. The offset is calibrated to 0.

It is possible to override the factory calibration by a user setting. Gain and offset in both AC and DC AFEs can be set individually for each channel by a user command. The user setting can be changed at any time.

2 Absolute Maximum ratings

Exposure to conditions exceeding these rating may reduce life time or permanently damage the device.

Table 1:

ABSOLUTE MAXIMUM RATINGS		
	Min	Max
Supply voltage (to GND)	–0.4 V	14 V
Analog input (AC)		4.4 V_{PP}
Trigger input (to GND)	–3 V	3.7 V
Clock input (AC)		3.3 V_{PP}
Ambient temperature (operation)	0 °C	45 °C

The ADQ214 has a built-in fan to cool the device. If the air flow is blocked or the fan malfunctions, the temperature surveillance unit will protect the ADQ214 from overheating by shutting down parts of the device.

The SMA connectors have an expected life time of 500 operations. For frequent connecting and disconnecting of cables, connector savers are recommended.

3 Architecture

3.1 Overview

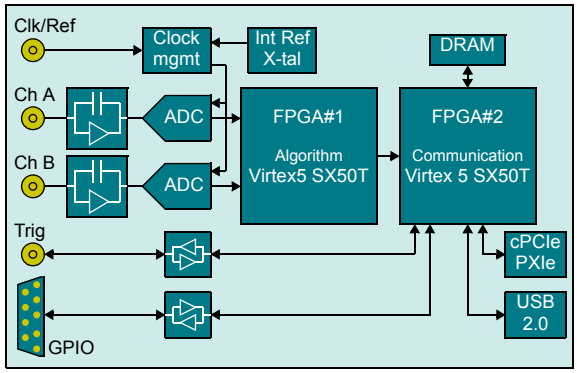


Figure 6: Block diagram

3.2 Analog Front End, AFE

The analog input is single ended 50 ohm. In the AC AFE, the single ended signal is converted to a differential signal in a balun. In the DC AFE, the single ended signal is buffered by a single ended to differential buffer.

3.3 ADC

The ADCs are 14 bit 400 MSps high precision ADCs.

3.4 Clock

3.5 Clock sources

The clock generator consists of a crystal oscillator as a clock reference and a PLL with built in VCO. The PLL has also built in dividers for generating necessary clock frequencies on the board. The sampling frequency is set by configuring these frequency dividers.

There is also an external SMA connector for either an external clock reference or an external clock source.

3.6 Setting the sample rate

There are several ways of setting the sample rate.

1. Setting the frequency in the PLL by adjusting the dividers.
2. Applying an external clock.
3. Applying an external reference. This is a fine tuning method, which is specially useful for locking several ADQ214 to the same frequency.
4. Using the sample skip function. The ADCs operate at full rate. The sample rate is set by selecting samples after the ADC. In this way, very low sampling rates be achieved. A long measurement times is enabled.
5. Using the decimation filter function, see **Section 3.11**.

3.7 FPGAs

The data outputs of the ADCs are connected to a first Xilinx XC5VSX50T-1 FPGA which is open for user applications through the ADQ214 Development Kit. The data is then transferred to a second FPGA, Xilinx XC5VSX50T-1, which handles the communication with the host and the batch data RAM. Parts of this FPGA is also open for user applications through the ADQ214 Development Kit.

3.8 Memory

There is 64 MSamples data batch memory per channel. The data batch length for each recording is set to any value within this range. For more information about memory handling, see **Section 3.10**.

3.9 Interface

The ADQ214 is connected to the host computer through a Hi-Speed USB interface which is used for control and uploading of data.

The USB connection can be configured in a streaming mode. The sustained data rate is then 25 MBytes/s[1]. This is typically used together with a data reduction algorithm, implemented through the ADQ214 Development Kit.

See **Section 5.1** for Compact PCI Express (cPCIe) / PXI Express (PXIe) interface.

3.10 Trigger

3.10.1 Overview

When armed, the system is waiting for the selected trigger event. At the trigger event, a data batch of selected length is recorded in the batch memory.

Pre-trigger buffer and trigger hold-off are available for control of the trigger position. The length of the pre-trigger buffer is set in number of samples[2]. The pre-trigger buffer is a part of the total batch length. The trigger hold-off is up to 2^{33} samples and is set in steps of 2 samples.

The ADQ214 has several trigger options, which are sumarized below. For a complete description of all the possible trigger settings, see the triggering application note 11-0701.

Software trigger, where data capture is triggered by a software command. This is suitable for measurements on continuous waves.

Level trigger, where data capture is triggered by an event on the input data. This is useful for capturing pulses. The level trigger combined with the pre-trigger or trigger hold-off setting can capture any pulse shape.

External trigger, where data capture is triggered by the edge on the trigger input connector. This is intended for synchronizing the signal source with the ADQ214. It can also be used for synchronizing multiple ADQ214 units.

1. This is highly dependent of other tasks performed by the operating system on the host computer.
2. There is a fixed amount of delay between the trigger and data depending on the length of the wires and the internal signal paths. This delay may change for a custom application using the ADQ214 Development Kit.

Internal trigger, where an internal timer generates triggers. The internat trigger jitter on the output pin is typically 50ps.

3.10.2 Trigger accuracy in the time domain

The trigger time accuracy is 625 ps, that is, one quarter of a sampling period. In **Figure 7** a set of asynchronous data batches are aligned using interpolation based on the accurate trigger to sub-sample timing precision.

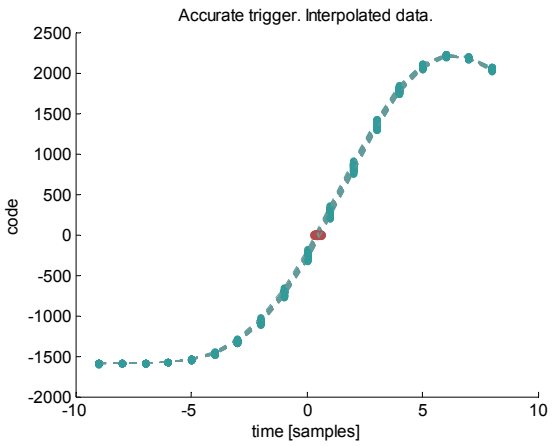


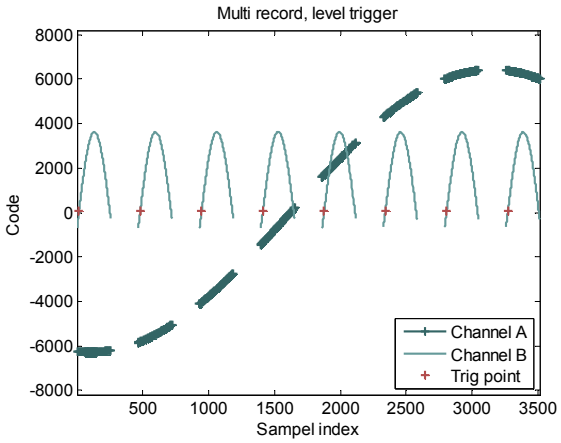
Figure 7: Aligned data

3.10.3 Multi record

The ADQ214 can be set up in a multi record mode. At each trigger, a record of data is recorded in the memory. The length of each record and number of records is user defined. Multi record works together with pre-trigger buffer and trigger hold off.

Figure 8 shows an example where a level trigger on channel B is used for triggering each record. Channel A samples a low frequency sine wave. The records have been reconstructed in time domain to illustrate the slow sine wave.

The pulse repeat frequency (PRF) can be set up to 1.6 MHz depending on the record length.



PRF	860	kHz
Record length	256	samples
Pre trig	16	samples
Trig level channel B	70	codes

Figure 8: Multi Record example

Table 2:

PULSE REPEAT FREQUENCY MULTI TRIG MODE	
Record length	Maximum PRF kHz (typ)
16	1600
64	1300
256	860
1024	340
4096	92
16384	24
65536	6.1

3.10.4 Time stamp

A 64 bits time counter, which runs on the sampling frequency, enables time stamp for each event. At each trigger event, the counter value is read and stored together with the data record.

The time counter starts at power up and may directly be used for relative time measurement. The counter can be reset by software. The counter can also be synchronized to an external start pulse. The external start pulse can operate in two modes; single start signal or repeated restart of the time counter. In the repeated restart mode, the counter is divided into a 42 bits time counter and a 22 bits start pulse counter.

The start pulse is connected to GPIO pin #2.

3.11 Decimation filter

A programmable decimation filter which can decimate up to 2^{34} times is available in the FPGA#1. Using the decimation filter is a way of reducing the sampling frequency and gain noise performance.

A decimation filter implements a close to ideal low pass filter, which suppresses the wide band quantization noise in digitizer. The theory of decimation gives that each factor of 4 in decimation yields one extra bit in resolution. The effect is an increased dynamic range.

The decimation filter makes the ADQ214 very flexible and a large set of measurement specifications can be met with the same device.

Table 3:

DECIMATION IP CONFIGURATIONS (EXAMPLES)		
Decimation order	Sampling rate	Resolution
$2^0 = 1$	400 MSps	14 bits
$2^4 = 16$	25 MSps	16 bits
$2^{12} = 4096$	98 kSps	20 bits

3.12 Averaging

The ADQ214 supports averaging. A set of records are accumulated in an accumulator. See application note 11-0699.

3.13 GPIO

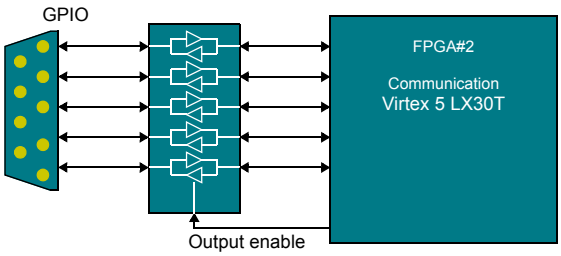
The ADQ214 is equipped with five bi-directional GPIOs with short circuit protection. The GPIOs are individually controlled from software, but can also be accessed from the ADQ214 Development Kit.

The connector is Micro D plug 9 way. A suitable socket with lead is for example MOLEX 83421-9044.

Pin #2 is also start signal for time stamp counter.

Pin#5 has a high drive capacity with only 30 ohms output impedance.

The trigger port can also be used as a bi-directional GPIO. The trigger can be configured as a trigger output, see **Figure 10**.



#	Function
1	GPIO
2	GPIO
3	GPIO
4	GPIO
5	GPIO
6	GND
7	GND
8	GND
9	GND

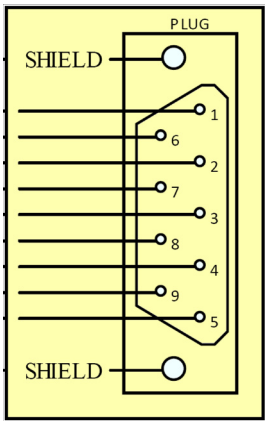


Figure 9: GPIO block diagram.

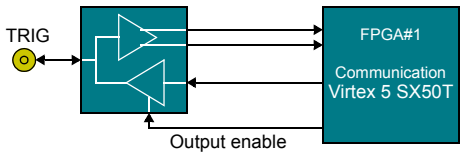


Figure 10: Trigger as GPIO: block diagram.

4 Software tools

4.1 ADCaptureLab

The ADQ214 is supplied with the ADCaptureLab software that provides quick and easy control of the digitizer. The tool also offers both time domain and frequency domain analysis, see **Figure 11**. Data can be saved in different file formats for off-line analysis. Comparison of results is easily done by importing data from file and analyze it in ADCaptureLab.

4.2 Software development kit (SDK)

The ADQ214 data acquisition system is easily integrated into your own application by using the included Software development kit. The SDK includes programming examples and reference projects for C/C++ and MATLAB.

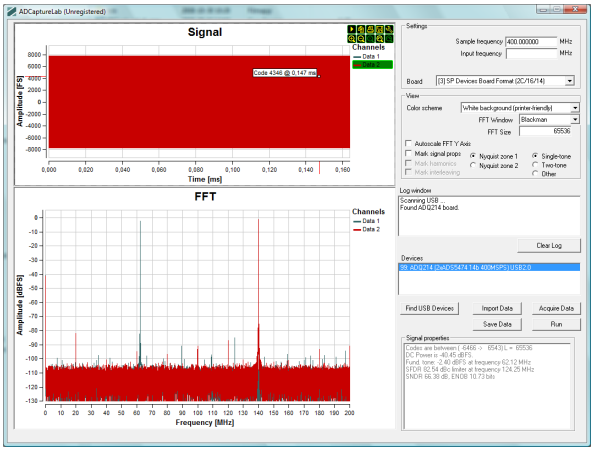


Figure 11: ADCaptureLab

5 Options

5.1 cPCIe / PXIe interface

The ADQ214 is available with cPCIe / PXIe interface. The ADQ214 supports Gen1 by 4 lanes.

Table 4:

cPCIe / PXIe INTERFACE		
Bus width	4	lanes
Bus peak capacity	8	Gbit/s
Sustained data rate, 4 lanes	790	MByte/s
PXIe card size	1 slot 3U 4TE	

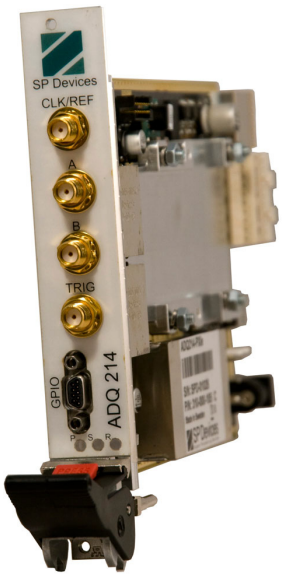


Figure 12: cPCIe / PXIe interface.

Order code: –PXIE

5.2 Biased AC coupled front end

For unipolar signals, a biased front-end is available. It places the zero level at a pre-biased level and the entire signal range can be used to measure the pulses.

A positive bias (for negative pulses) is available at 90% of the signal range.

Order code: –PB

A negative bias (for positive pulses) is available at 10% of the signal range.

Order code: –NB

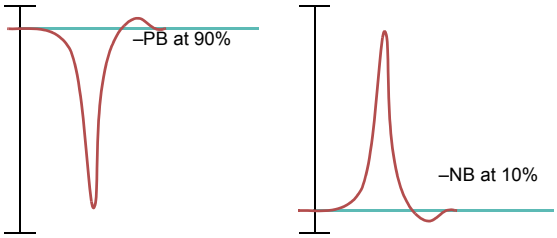


Figure 13: Bias option

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www.spdevices.com

Teledyne SP Devices Corporate Headquarters

Teknikringen 6
SE-583 30 Linköping
Sweden

Phone: +46 (0)13 465 0600
Fax: +46 (0)13 991 3044
Email: info@spdevices.com