ADQ32-PDRX Datasheet

The ADQ32-PDRX is a high-speed digitizer with extended dynamic range for pulse data applications. The ADQ32-PDRX features:

- **One analog input channel**
- **12 bits resolution**
- **3 bits dynamic range extension through built-in dual-gain channel combination**
- **2.5 GSPS sampling rate**
- **7 GByte/s sustained data transfer rate to GPU**
- **7 GByte/s sustained data transfer rate to CPU**
- **Two external triggers**
- **General Purpose Input/Output (GPIO)**
- **Open FPGA for real-time signal processing**
- **Firmware option for averaging of records**
- **Firmware option for pulse analysis**

1 ORDERING INFORMATION

ADQ32-PDRX is available with a set of options. Follow the procedure to configure the ADQ32. Start with the hardware configurations. These are factory installed and cannot be changed through software commands.

1. Dual-gain channel-combination analog front-end **-PDRX** is included on ADQ32-PDRX. For standard DC-coupled analog front-end, see 20-2378 ADQ32 datasheet.
2. PCIe interface is standard.

Select the firmware options. The firmware FWDAQ is always included. Additional firmware files are distributed as files and can be loaded into the board at any time.

3. Data acquisition firmware **-FWDAQ** is always included
4. Select one or several of available firmware packages, **-FWATD**, **-FWPD**.
5. On-board channel combination for dual-gain pulse detection is included on ADQ32-PDRX for all firmware options.
6. Select accessories, open FPGA development kit **DEVDAQ**, **DEVPD**[1].
7. Select extended warranty **-W5Y**.

The open FPGA is accessed through the design project for each firmware. For **-FWDAQ**, the development kit is **DEVDAQ**. For **-FWPD**, the development kit is **DEVPD**. The **DEVDAQ** is a one-time purchase. The FPGA bit files built from the design project can be used on any ADQ32 with a valid FWDAQ license (included on all units).

[1] DEVPD is available in 2024. Contact Teledyne SP Devices for more information.

2 ADQ32-PDRX INTRODUCTION

2.1 Features

- One input channel
- 2.5 GSPS sampling rate
- 12 bits resolution
- 3 bits dynamic range extension through built-in dual gain channel combination
- DC-coupled with 760 MHz bandwidth
- Programmable DC offset
- Internal and external clock reference
- Internal and external sampling clock
- Clock reference output
- Internal and external triggers
- 8 Gbytes data memory
- 7 Gbyte/s sustained data streaming to CPU and GPU
- Data interface PCIe Gen3 x8
- Averaging firmware FWATD
- Pulse analysis firmware FWPD

2.2 Applications

- Time-of-flight mass spectrometry
- LIDAR
- Pulse data systems

2.3 Advantages

- ADQ32-PDRX integrates the analog dual-gain amplifier for a compact high-performance system solution
- Real-time processing for pulse data capture and high data throughput
- Teledyne SP Devices' design services are available for fast integration to reduce time-to-market

2.4 System design optimization; open FPGA and streaming to CPU and GPU

High-performance data acquisition systems require high speed real-time analysis. ADQ32-PDRX uses a built-in dual-gain channel combination to increase the dynamic range in pulse capture. Weak pulses are captured through a channel with high gain and strong pulses are captured through a channel with low gain. The channel combination results in a dynamic range extension equivalent to 3 extra bits of vertical resolution.

The PDRX channel combination is carried out by the digitizer firmware and is available for **FWATD**, **FWPD** and **FWDAQ**.

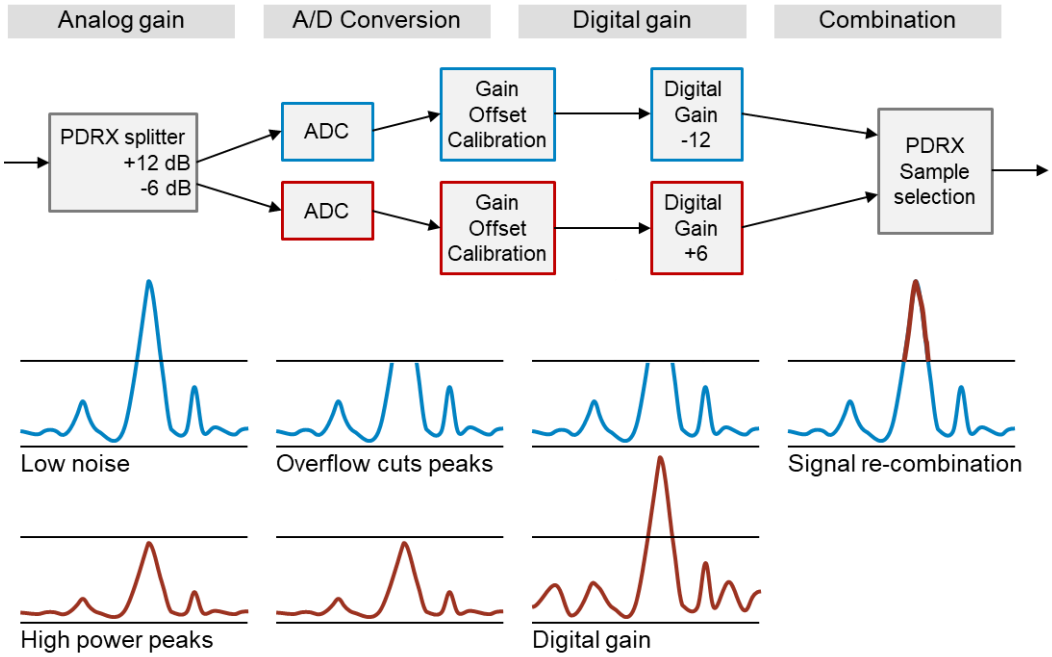


Figure 1 Principle of channel combination

The ADQ32-PDRX hardware can also be used for custom channel combination. The combination firmware is then bypassed, and the board operate with 2 channels output.

In addition to the specific pulse detection, ADQ32-PDRX supports a variety of options for efficient system design:

Streaming to GPU
ADQ32-PDRX supports up to 7 GByte/s peer-to-peer streaming and streaming via pinned buffer to GPU. A GPU offers a powerful platform for implementing application-specific signal processing algorithms.

Streaming to CPU
ADQ32-PDRX supports up to 7 GByte/s to host computer. Implementing the application-specific algorithms in the CPU results in an efficient system.

Open FPGA for real-time processing
ADQ32-PDRX offers an open FPGA for implementation of the application-specific computations in the FPGA. This gives the most compact system design. Firmware development kit is ordered separately.

3 TECHNICAL DATA

Technical parameters are valid for ADQ32-PDRX operating with firmware FWDAQ. All parameters are typical unless otherwise noted.

Table 1 Analog input (front panel label A)

Parameter	Condition	Min	Typical	Max	Unit
Basic parameters					
Number of channels			1		
Sampling rate			2.5		Gsample/s
Bandwidth	-3dB		760		MHz
Input range			1		Vpp
Input impedance			50		Ω
Coupling			DC		
Connector type			SMA		
Programmable DC-offset					
DC-offset range		-0.5		+0.5	V
Dynamic performance					
Idle channel noise[2]			71		dBFS
ENOB noise based[3]			11.6		bits

Table 2 Comparison of ADQ32-PDRX to ADQ32

Parameter	Condition	ADQ32	ADQ32-PDRX	Unit
RMS noise	Terminated input	244	96	µV
Max input range		0.5	1	Vpp
DC-offset		-0.25 to 0.25	-0.5 to 0.5	V
Dynamic range[4]		57.2	71.3	dB
ENOB[5]		9.2	11.6	bits
Bandwidth	-3dBFS	1000	760	MHz
Attenuation at 1GHz		3	5.1	dB

[2] Measured integrated noise with a terminated input. Noise level is computed relative a full-scale sine wave.
[3] Computed from idle channel noise. See figure for ENOB at sweep of input power.
[4] Power of full-scale sine wave relative noise with terminated input.
[5] Computed from “Dynamic Range” in

Table 2 using the formula (Dynamic Range – 1.76) / 6.02.

Table 3 Clock generator and front panel CLK connector.

Parameter	Condition	Min	Typical	Max	Unit
Internal clock reference					
Frequency			10		MHz
Accuracy			±3 ±1/year		ppm
Internal sampling clock generator [6]					
Frequency range 1		2440	2500	2500[7]	MHz
Frequency range 2		1840		1970	MHz
External clock reference input (from front panel CLK connector)[8]					
Frequency		1	10	500	MHz
Frequency [9]	Jitter cleaner enabled	10 -10 ppm	10	500 +10 ppm	MHz
Frequency	Delay line used		10	100	MHz
Delay line tuning range[10]			500		ps
Signal level		0.5		3.3	Vpp
Input impedance	AC		50		Ω
Input impedance	DC		10k		Ω
Input impedance (high) [11]	AC		200		Ω
Clock reference output (on front panel CLK connector)[12]					
Frequency			10		MHz
Signal level	Into 50-Ω load		1.2		Vpp
Output impedance	AC		50		Ω
Output impedance	DC		10k		Ω
External direct sampling clock input (from front panel CLK connector)[13]					
Frequency [14]		1000		2505	MHz
Signal level		0.5		3.3	Vpp
Impedance	AC		50		Ω
Impedance	DC		10k		Ω
Physical connector label CLK					
Connector type		SMA			

[6] The internal clock generator can generate frequencies in 2 different ranges.
[7] The software setting limit. The tolerance with external clock reference is up to 2505 MHz.
[8] Using a clock reference from an external source to synchronize the ADQ32 to the external source.
[9] The jitter cleaner requires the reference frequency to be a multiple of 10 MHz within ± 10ppm.
[10] Tuning of sampling clock phase relative to external clock reference input phase.
[11] Software-selectable high-impedance mode.
[12] The internal clock reference of the ADQ32-PDRX is made available to synchronize external equipment.
[13] Using an external clock while bypassing the internal clock generator.
[14] In single-channel mode, the sampling frequency is 2 times the external clock frequency.

Table 4 Front panel TRIG connector

Parameter	Condition	Min	Typical	Max	Unit
Connector type		SMA			
Used as input (or GPIO)					
Impedance	DC		50		Ω
Impedance (high) [15]	DC		500		Ω
Signal level	50-Ω mode	-0.5		3.3	V
Adjustable threshold	50-Ω mode	0		2.8	V
Signal level	High impedance	-0.5		5.5	V
Adjustable threshold	High impedance	0		2.3	V
Pulse repetition frequency	As trigger			10	MHz
Time resolution [16]	As trigger		50		ps
Update rate [16]	As GPIO			156.25	MHz
Used as output (or GPIO)					
Impedance	DC		50		Ω
Output level high VOH	Into 50-Ω load	1.8			V
Output level low VOL	Into 50-Ω load			0.1	V
Pulse repetition frequency				156.25	MHz

Table 5 Front panel SYNC connector (may be used as a trigger source with larger timing grid)

Parameter	Condition	Min	Typical	Max	Unit
Connector type			SMA		
Used as input (or GPIO)					
Impedance	DC		50		Ω
Impedance (high) [15]	DC		500		Ω
Signal range	50-Ω mode	-0.5		3.3	V
Adjustable threshold	50-Ω mode	0		2.8	V
Signal level	High impedance	-0.5		5.5	V
Adjustable threshold	High impedance	0		2.3	V
Pulse repetition frequency	As trigger			10	MHz
Time resolution [16]	As trigger		3.2		ns
Update rate [16]	As GPIO			156.25	MHz
Used as output (or GPIO)					
Impedance	DC		50		Ω
Output level high VOH	Into 50-Ω load	1.8			V
Output level low VOL	Into 50-Ω load			0.1	V
Pulse repetition frequency				156.25	MHz

[15] Software-selectable high-impedance mode.

[16] Timing properties are valid for 2.5 GSPS in 2 channel mode and 5 GSPS in 1 channel mode. Timing properties scale linearly with sampling frequency.

Table 6 Front panel GPIO connector

Parameter	Condition	Min	Typical	Max	Unit
Connector type			SMA		
Used as input					
Impedance			50		Ω
Impedance (high) [15]			10		kΩ
Input level high VIH		2			V
Input level low VIL				0.8	V
Update rate [16]				156.25	MHz
Used as output					
Output Impedance			50		Ω
Output level high VOH	Into 50-Ω load	1.5			V
Output level high VOH	No load	3.2			V
Output level low VOL	Into 50-Ω load			0.1	V
Output level low VOL	No load			0.1	V
Update rate [16]				156.25	MHz

Table 7 Custom GPIO expansion. See section 0.

Parameter	Value
Connector type	40-pin FFC/FPC connector, pitch 0.5 mm
Number of differential IO signals LVDS	8
Number of single-ended IO signals 3.3V	5

Table 8 Environment and mechanical parameters

Parameter	Condition	Min	Typical	Max	Unit
Power and temperature					
Power consumption [17]	FWDAQ		30		W
Power supply		10.8	12	13.2	V
Operating temperature	At fan inlet	0		45	°C
Size					
Width			1		slot
Length			225.7		mm
Height			111.2		mm
Compliances					
RoHS3		Yes			
CE		Yes			
FCC	Exclusion according to CFR 47, part 15, paragraph 15.103(c).				

[17] Power consumption depends on firmware option and use case. Power consumption is measured during acquisition and streaming of data at 5 Gbyte/s to PC.

Table 9 Data acquisition

Parameter	Condition	Min	Typical	Max	Unit
Rearm time[18]				20	ns
Acquisition memory (Data FIFO)	Shared by all channels		8		Gbyte
Record length	2 channels mode	16		2^{32}-1	samples
	Combined channels	16		2^{32}-1	samples
Pretrigger[19]	2 channels mode in steps of 8	8		16 360	samples
	Combined in steps of 8	8		16 360	samples
Trigger delay[20]	2 channels mode in steps of 8	8		2^{35}-8	samples
	Combined in steps of 8	8		2^{35}-8	samples

Table 10 Data transfer

Parameter	Value	Unit
Supported versions of data transfer standard PCIe	Gen1 / Gen2 / Gen3	
Supported number of lanes[21]	1 / 4 / 8	
Data rate to CPU sustained with headers	5	GByte/s
Data rate to CPU sustained without headers	7	GByte/s
Data rate to GPU sustained without headers	7	GByte/s
Data rate peer-to-peer to GPU sustained without headers	7	GByte/s

Table 11 Software support

Parameter	Value
Operating system[22]	Windows Linux
GUI	Digitizer Studio
Example code	C, Python
API	C / C++

[18] Minimum time from the last sample of a record to the next trigger.
[19] Pre-trigger is set by assigning the parameter “horizontal offset” a negative value
[20] Trigger delay is set by assigning the parameter “horizontal offset” a positive value
[21] The ADQ30 must be installed in a 16 lanes slot or a slot with a connector with an open end.
[22] See 15-1494 Operating system support for a detailed listing of supported distributions.

4 FEATURES FOR DATA FLOW CONTROL, SYNCHRONIZATION AND PROCESSING

The ADQ32-PDRX features an advanced machine for flow control, synchronization, and signal processing. The block diagrams are shown in Figure 2 and Figure 3. The features are described in the following tables.

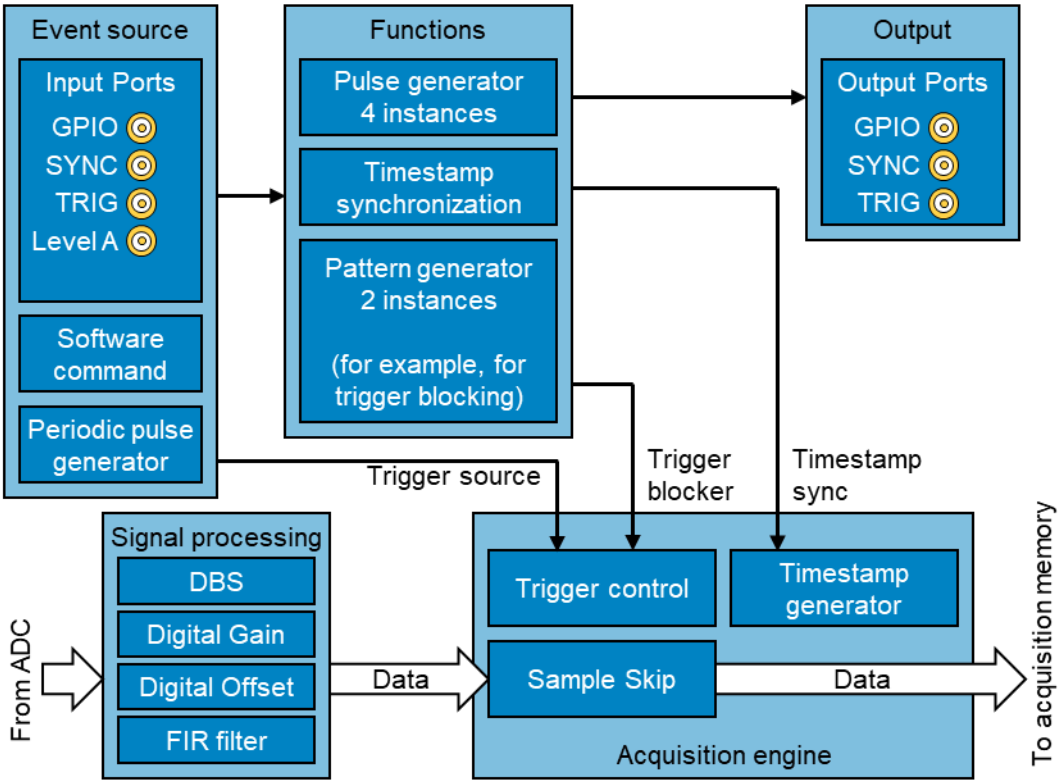


Figure 2 Flow control and synchronization block diagram.

Table 12 Digital signal processing blocks

Object type	Available selections
Digital Signal Processing Included signal processing in the data path for enhanced signal quality.	Digital Baseline Stabilizer (DBS) Digital gain Digital offset Digital FIR filter

Table 13 Flow control blocks

Object type	Available selections
Input ports Electrical connections to the ADQ32 for real-time operation (excluding the PCIe data interface) Used as event source.	Front panel TRIG Front panel SYNC Front panel GPIO Front panel CLK (clock reference or clock input only) Analog channel A
Event sources Signals for real-time control of activities in the firmware of ADQ32.	Software command External TRIG External SYNC External GPIO Internal periodic event generator Level analog channel
Functions Included operations for real-time control of activities in the firmware of ADQ32.	Pattern generator for timestamp synchronization Pattern generator general purpose, 2 instances Pulse generator, 4 instances
Output ports Electrical connections to the ADQ32 for real-time operation (excluding the PCIe data interface).	Front panel TRIG Front panel SYNC Front panel GPIO Front panel CLK (clock reference output only)

Table 14 Firmware functions for flow control

Function	Modes/selections	Event sources as stimuli
Pattern generator for timestamp synchronization Control the time of the ADQ32-PDRX.		Software command External TRIG External SYNC Internal periodic event generator
Pulse generator Control output pulse shapes. Three instances.	Rising edge Falling edge Pulse length Polarity	Software command External TRIG External SYNC Internal periodic event generator
Pattern generator general purpose For example, used for trigger blocking.	Once Window Gate Trigger counter	Software command External TRIG External SYNC Internal periodic event generator

Table 15 Firmware functions for acquisition

Function	Modes	Event Sources as stimuli / control
Trigger Initiate the acquisition of a data record.		Software command External TRIG External SYNC Internal periodic event generator Level analog channel A
Data acquisition modes Configurations for sending digital data to the host PC.	Fixed record length Dynamic record length (zero suppression)	Selected **Trigger**
Data transfer modes Transport to CPU / GPU	Streaming with header Streaming without header	User set-up

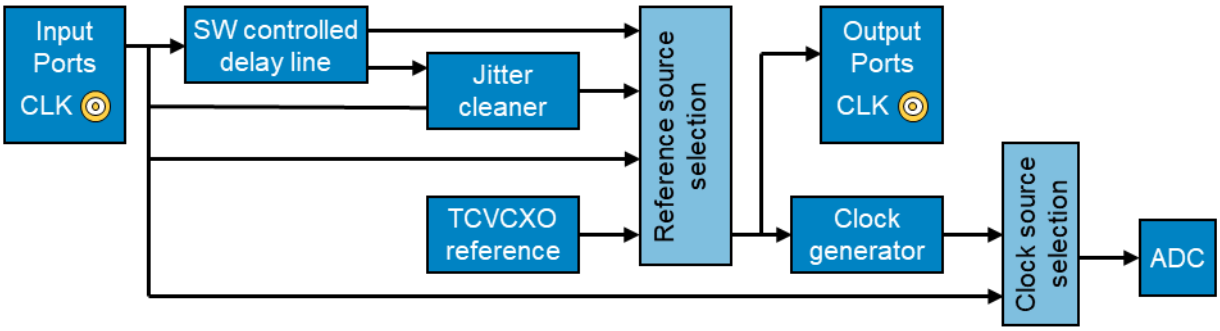


Figure 3 Clock generation block diagram.

Table 16 Clock generation

Function	Modes
Clock reference source Phase and frequency reference for the clock system.	Internal External External with jitter cleaner and/or delay line
Sampling clock sources Actual clock for taking the samples of the analog data.	Internal clock generator Direct external clock
Clock output	Selected clock reference

5 FIRMWARE

5.1 FWDAQ

The FWDAQ is included with all digitizers. The firmware includes control of the hardware and recording of data.

The channel combination is included in FWDAQ for ADQ32-PDRX hardware.

5.2 FWATD

The FWATD is optional. It includes thresholding for noise suppression and accumulations of waveforms. See datasheet 22-2912 for more details.

The channel combination is included in FWATD for ADQ32-PDRX hardware.

5.3 FWPD

The FWPD is optional. It includes detection and analysis of pulses. See datasheet 23-3028 for more details.

The channel combination is included in FWPD for ADQ32-PDRX hardware.

5.4 Managing firmware

The digitizer supports multiple firmware images. Note the following about managing firmware images:

- The non-volatile memory on the digitizer can store up to four different firmware images (including the active firmware). Use the tool ADQAssist to change firmware and to upload new images to the digitizer.
- Each hardware can include a license for multiple firmware options. If all firmware images cannot be stored on the device, some may need be stored on the host computer for manual reprogramming via ADQAssist.
- The digitizer (and the enclosing host computer) must be power cycled for the firmware switch to be completed. This is required to let the PCIe bus enumerate with the new firmware.
- Some firmware features require a valid license key to activate. See the ordering information section for details about available firmware features.

6 ABSLOUTE MAXIMUM RATINGS

Table 17 Absolute maximum ratings

Parameter	Condition	Min	Max	Unit
Power supply to GND		-0.4	14	V
Operating temperature		0	45	°C
Analog in to GND Peak		-7	+7	V
Analog in to GND DC		-3	+3	V
TRIG to GND	50-Ω mode	-2	5	V
SYNC to GND	50-Ω mode	-2	5	V
TRIG to GND	500-Ω mode	-2	6	V
SYNC to GND	500-Ω mode	-2	6	V
CLK REF to GND AC amplitude			5	Vpp
CLK REF to GND DC-level		-5	5	V
GPIO to GND		-1.5	5	V
FFC / FPC differential signal to GND	Powered[23]	-0.5	2.3	V
	Not powered[23]	-0.5	0.5	V
FFC / FPC single-ended signal to GND [23]	Powered[23]	-0.3	3.8	V
	Not powered[23]	-0.3	0.5	V

Exposure to conditions exceeding these ratings may reduce lifetime or permanently damage the digitizer. The digitizer with PCIe format has a built-in fan to cool the device. The built-in temperature monitoring unit will protect the digitizer from overheating by temporarily shutting down parts of the device in an overheat situation.

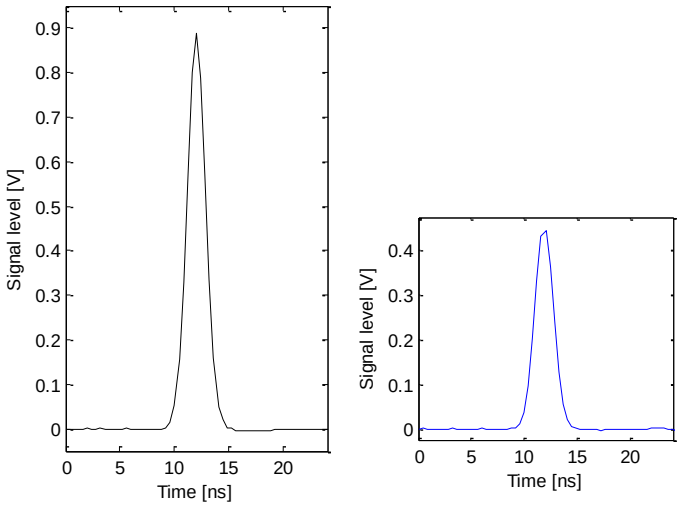
The SMA connectors have an expected lifetime of 500 operations. For frequent connecting and disconnecting of cables, connector savers are recommended.

[23] The absolute maximum ratings depend on whether the ADQ32-PDRX is powered or not. It is recommended to use the respective power rail in the FFC connector to power or enable the external drivers to avoid driving overvoltage into an unpowered digitizer. Use the 1.8 V rail for the differential signals and 3.3 V for the single-ended signals.

7 TYPICAL PERFORMANCE

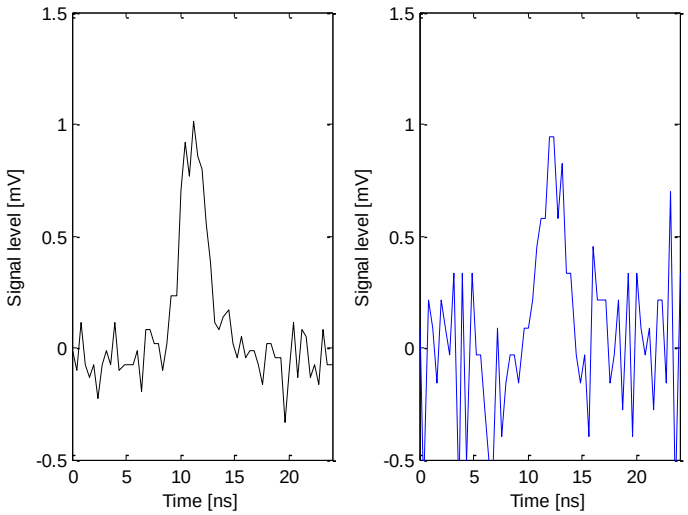
7.1 Time domain pulse data

Pulse examples of different amplitude are plotted showing a ratio of 1000 : 1. The pulses are compared with ADQ32 for reference to illustrate the benefit of ADQ32-PDRX in this application. Notice that other applications may benefit from the properties of ADQ32 instead.



(a) ADQ32-PDRX (b) ADQ32

Figure 4 Time domain plot of pulses at 90% of full-scale for the respective digitizer. Notice that ADQ32-PDRX can accept larger signals without overrange



(a) ADQ32-PDRX (b) ADQ32

Figure 5 Time domain plot pulse at 0.9 mV. Notice that the pulse is easier to detect in the ADQ32-PDRX which has lower noise than the ADQ32.

7.2 Time domain pulse accuracy

Pulse amplitude accuracy for the combined signal is measured in amplitude sweep.

This is a measurement of the static gain. The amplitude measurement of a wide pulse is related to the input signal amplitude. The deviation form the expected value in percent relative signal level and relative full scale is shown.

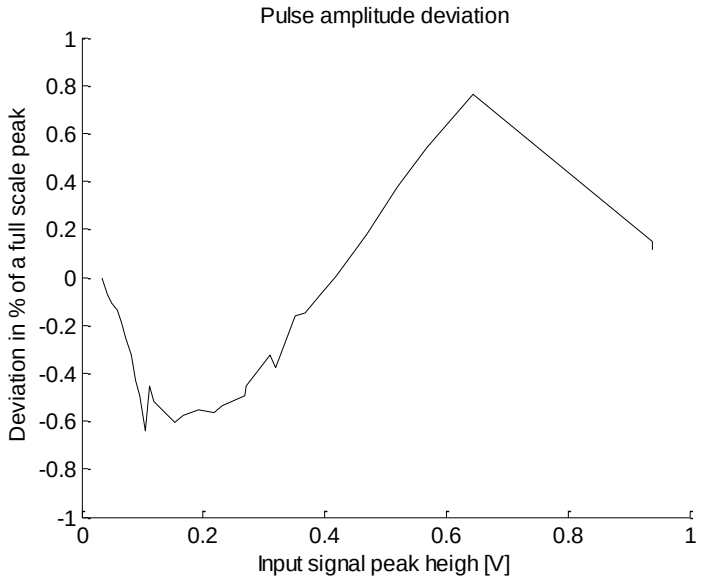


Figure 6 Deviation from ideal pulse height relative to full-scale pulse.

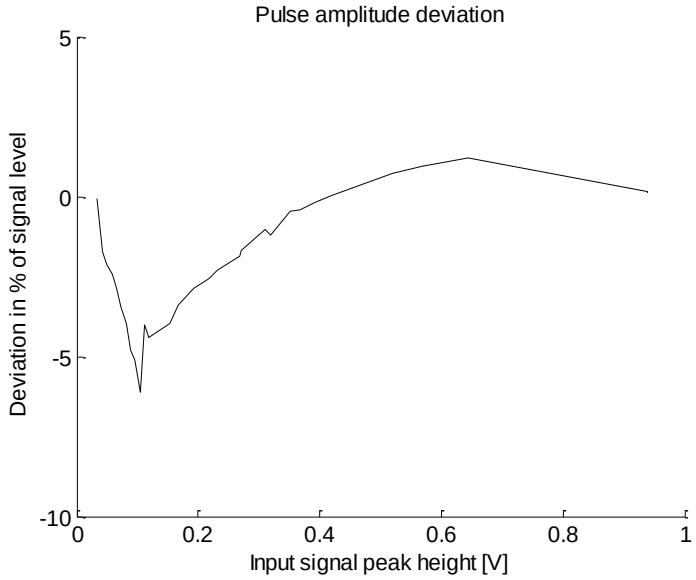


Figure 7 Deviation from ideal pulse height relative pulse level.

7.3 Timing accuracy

The timing between the branches is measured for frequencies and temperature for 4 units and shown in Figure 8.

A narrow band signal is injected at the input. The phase of the two branches is compared for different frequencies and different ambient temperature. The phase is converted to time difference. This means that pulses in the high gain branch and the low gain branch differ less than 13 ps in time for all 4 boards over temperature.

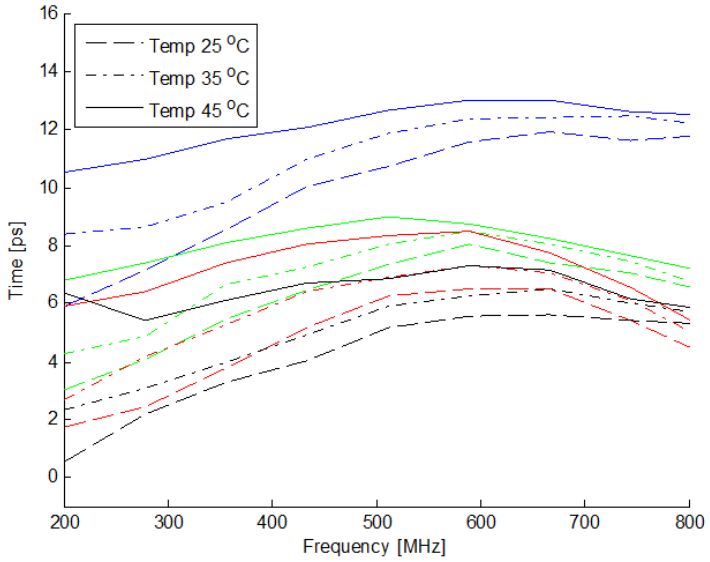


Figure 8 Time difference between branches for 4 units over temperature and frequency.

7.4 Frequency response

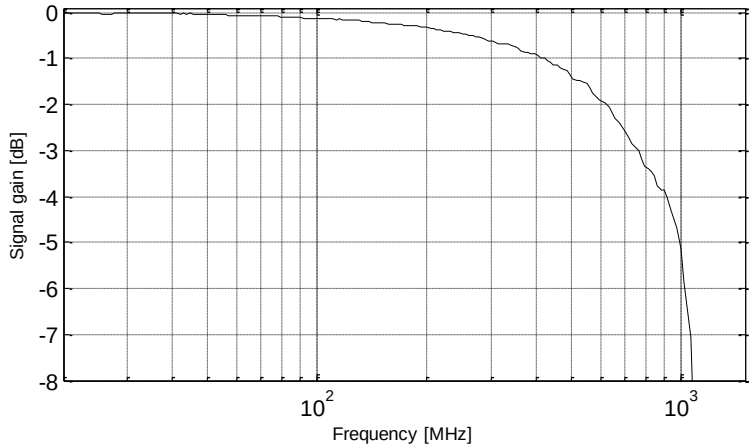


Figure 9 Frequency response, typical performance.

8 BLOCK DIAGRAM

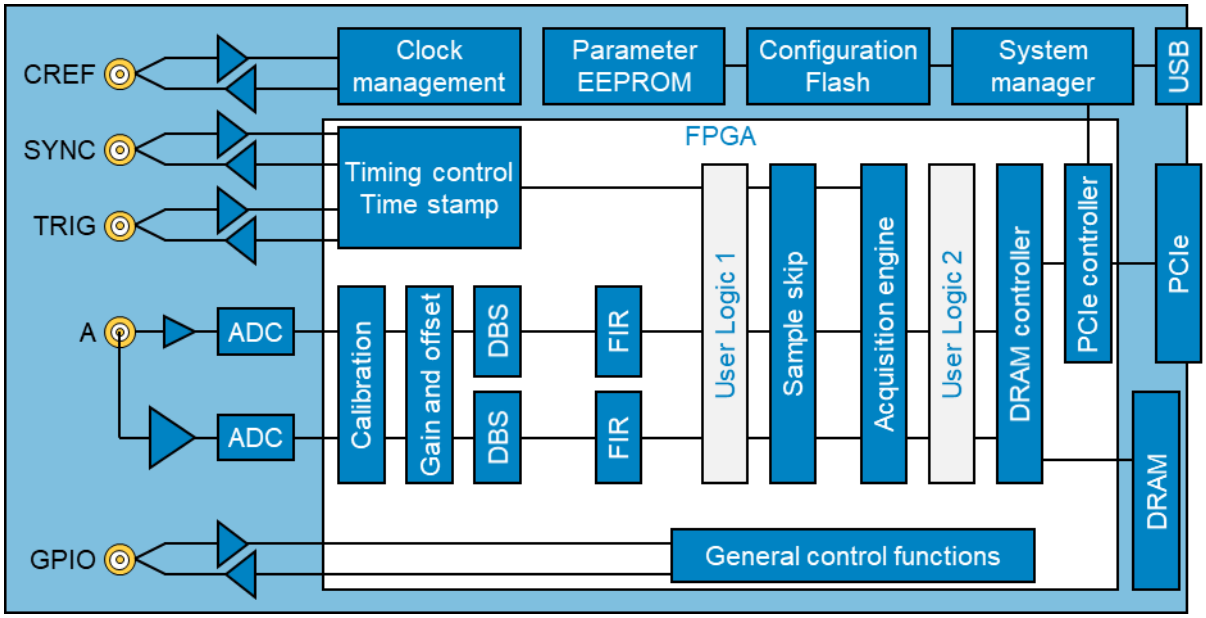


Figure 10 Block diagram ADQ32-PDRX-FWDAQ-PCIe bypass channel combination

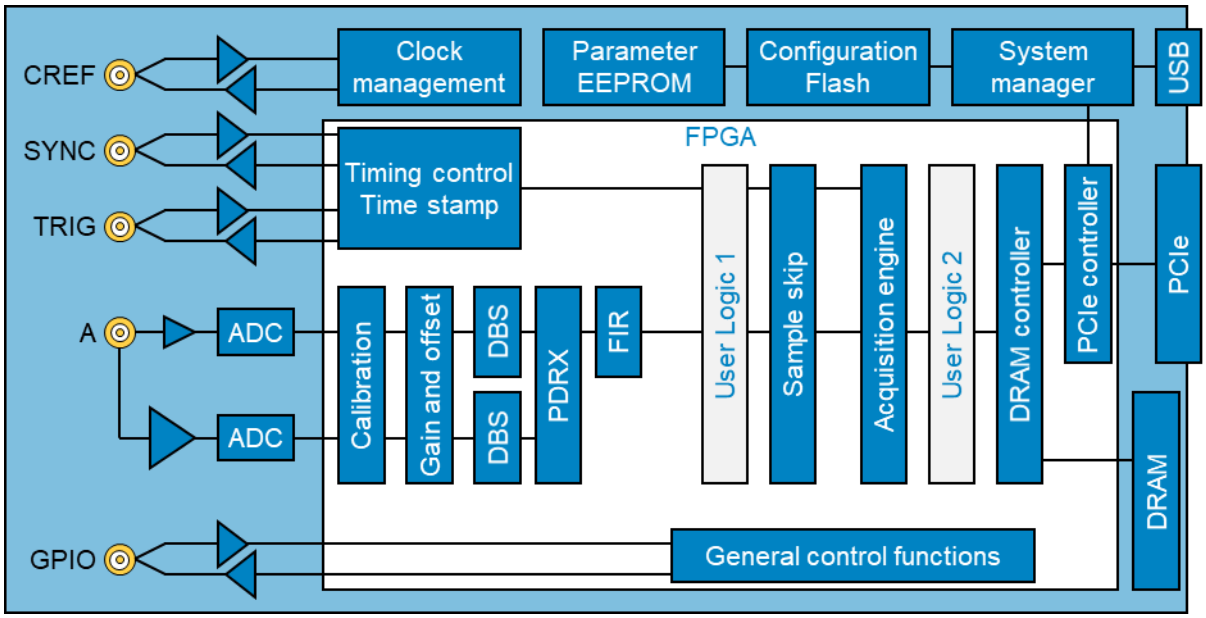


Figure 11 Block diagram ADQ32-PDRX-FWDAC-PCIe

Figure 10 shows a block diagram of ADQ32-PDRX using FWDAQ when the channel combination is bypassed. The two signals with different gain are passed to the user for channel combination.

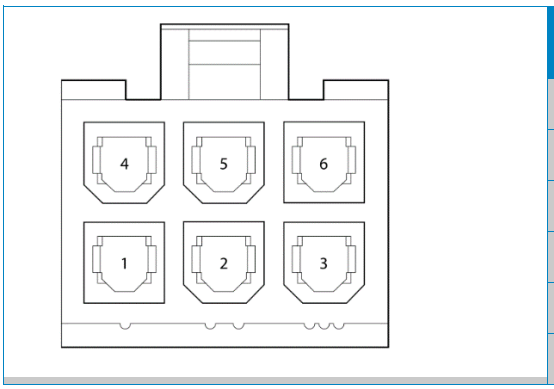
Figure 11 shows a block diagram of ADQ32-PDRX using FWDAQ including channel combination. There is only one output channel.

The boxes “User Logic” are open for custom real-signal processing thought the firmware development kit (purchased separately).

9 HOST PC INTERFACE PCIE

The ADQ32-PDRX-PCIe is powered from the power supply of the PC via a PCI Express 6-pin (2x3) auxiliary power supply connector. The connection in the cable should be as in Figure 12. A suitable connector is for example Molex 45559-0002.

It is important that the auxiliary power supply is turned on immediately when the PC starts. Otherwise, the digitizer will not be recognized on the PCI Express bus.



Pin	Signal
1	+12 V
2	+12 V
3	+12 V
4	Ground
5	Sense (Ground)
6	Ground

Figure 12 Power supply connection. Cable connector, looking into the connector end.

10 GPIO EXPANSION

The FFC connector allows direct access to the FPGA for building custom expansion boards. The FFC connector requires custom firmware and is accessible through the FPGA development kit. The ADQ32-PDRX user guide document number 21-2539 contains a description of connector.

Note that this connector is connected directly to the FPGA. Damage caused by custom hardware failure is not covered by warranty.

Contact Teledyne SP Devices' sales representative for more information.

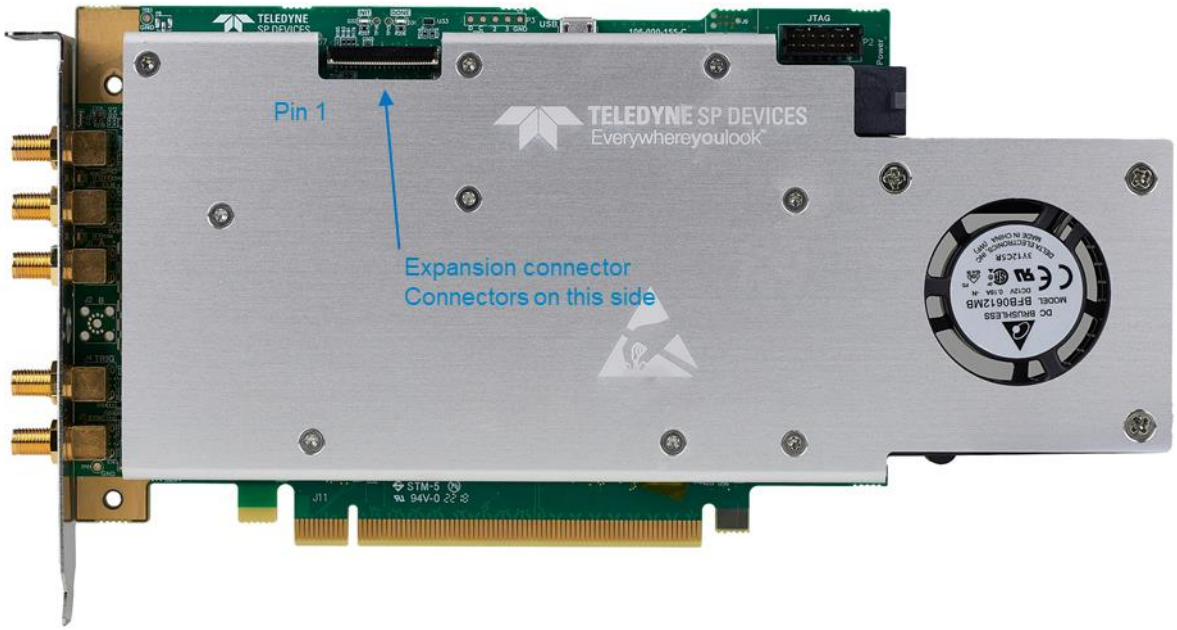


Figure 13 ADQ32-PDRX photo showing GPIO expansion connection on the top side.

11 MECHANICAL DRAWING

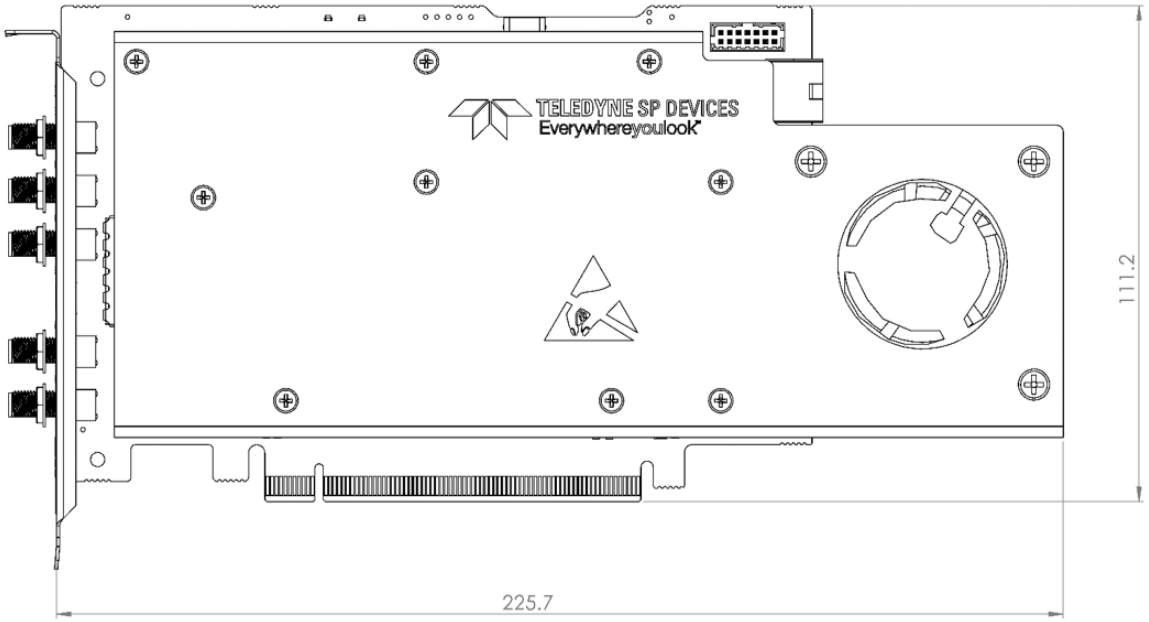


Figure 14 Mechanical drawing

12 REFERENCES

Refer to TSPD's web site spdevices.com for the latest version of documents.

15-1494 Supported operating systems

18-2059 ADQUpdater user guide

20-2378 ADQ32 datasheet

20-2507 ADQ3 series development kit user guide

20-2521 ADQAssist user guide

21-2539 ADQ3 series user guide

22-2912 ADQ3 FWATD datasheet

23-3028 ADQ3 FWPD datasheet

Important Information

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