ADQ33 Datasheet

The ADQ33 is a high-end 12-bit dual-channel data acquisition board optimized for use in high-throughput scientific applications. The ADQ33 features:

- **Two analog channels**
- **1 GSPS per channel**
- **12 bits resolution**
- **7 GByte/s sustained data transfer rate to GPU**
- **7 GByte/s sustained data transfer rate to CPU**
- **Two external triggers**
- **General Purpose Input/Output (GPIO)**
- **Open FPGA for real-time signal processing**
- **Firmware option for averaging of records**
- **Firmware option for pulse analysis**

1 ORDERING INFORMATION

ADQ33 is available with a set of options. Follow the procedure to configure the ADQ33. Start with the hardware configurations. These are factory installed and cannot be changed through software commands.

1. The two channel DC-coupled analog front-end is standard. For dual-gain **-PDRX** analog front-end, see datasheet 23-3042.
2. PCIe interface is standard.

Select the firmware options. The firmware FWDAQ is always included. Additional firmware files are distributed as files and can be loaded into the board at any time.

3. Data acquisition firmware **-FWDAQ** is always included
4. Select any set of available firmware packages, **-FWATD**, **-FWPD**.
5. Select to activate channel combination option for dual-gain pulse detection, **-LICPDRX**[1].
6. Select accessories, open FPGA development kit **-DEVDAQ**, **-DEVPD**[2].
7. Select extended warranty **-W5Y**[3].

The open FPGA is accessed through the design project for each firmware. For **FWDAQ**, the development kit is **DEVDAQ**. For **FWPD**, the development kit is **DEVPD**. The development kits are a one-time purchase. The FPGA bit files built from these design projects can be used on any ADQ33 with a valid corresponding firmware license.

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[1] See 23-3042 ADQ33-PDRX datasheet 23-3042 for more information about dual-gain channel combination. The ADQ33 can be used with external dual-gain amplifier and channel combination in firmware. The option LICPDRX activates the channel combination for external dual-gain amplifier.
[2] DEVPD is available in 2024. Contact Teledyne SP Devices for more information.
[3] Included warranty is 3 years from the date the product is shipped by Teledyne SP Devices. This option extends the warranty to 5 years from the date the product is shipped by Teledyne SP Devices. Warranty extension must be ordered before the included 3 years warranty is expired.

2 ADQ33 INTRODUCTION

2.1 Features

- Two analog input channels
- 1 GSPS sampling rate per channel
- 12 bits resolution
- DC-coupled with 1 GHz bandwidth
- Programmable DC offset
- Internal and external clock reference
- Internal and external sampling clock
- Clock reference output
- Internal and external triggers
- 8 Gbyte data memory
- 7 GByte/s sustained data streaming to CPU and GPU
- Data interface PCIe Gen3 x8
- Averaging firmware FWATD
- Pulse analysis firmware FWPD

2.2 Applications

- Swept-Source Optical Coherence Tomography (SS-OCT)
- Time-of-flight mass spectrometry
- Distributed Optical Fiber Sensing
- LIDAR
- Scientific instruments
- Scanning acoustic microscopy

2.3 Advantages

- A compact high-performance digitizer that optimize the system solution
- Real-time processing and high data throughput
- Teledyne SP Devices' design services are available for fast integration to reduce time-to-market

2.4 System design optimization; open FPGA and streaming to CPU and GPU

High-performance data acquisition systems require high speed real-time analysis. ADQ33 offers a variety of options for efficient system design:

Streaming to GPU
ADQ33 supports up to 7 GByte/s peer-to-peer streaming and streaming via pinned buffer to GPU. A GPU offers a powerful platform for implementing application-specific signal processing algorithms.

Streaming to CPU
ADQ33 supports up to 7 GByte/s to host computer. Implementing the application-specific algorithms in the CPU results in an efficient system.

Open FPGA for real-time processing
ADQ33 offers an open FPGA for implementation of the application-specific computations in the FPGA. This gives the most compact system design. Firmware development kit is ordered separately.

Pulse data recording
The hardware option ADQ33-PDRX offers a built-in dual-gain amplifier for pulse data capture with extended dynamic range. See 23-3042 ADQ33-PDRX datasheet for more details on the option.

3 TECHNICAL DATA

Technical parameters are valid for ADQ33 operating with firmware FWDAQ. All parameters are typical unless otherwise noted.

Table 1 Analog input (front panel label A and B)

Parameter	Condition	Min	Typical	Max	Unit
Basic parameters					
Number of channels			2		
Sampling rate per channel			1		GSample/s
Bandwidth -3dB			1		GHz
Input range			0.5		Vpp
Input impedance			50		Ω
Coupling			DC		
Connector type		SMA			
Programmable DC-offset					
DC-offset range		-0.25		+0.25	V
Dynamic performance					
Cross talk	< 500 MHz		-70		dBFS
Noise power density	0 to 500 MHz		-144		dBFS/√Hz
SNR	0 to 500 MHz, -1dBFS		55		dBc
SFDR	0 to 500 MHz, -1dBFS		64		dBc
ENOB relative full scale	0 to 500 MHz, -1dBFS		8.9		bits
Dynamic performance using FIR filter[4]					
SNR	110 MHz, -1dBFS		57		dBc
ENOB relative full scale	110 MHz, -1dBFS		9.4		bits

[4] Built-in user-programmable digital FIR filter; symmetrical, 17 taps. Filter coefficients used for this test are [57, 92, –279, 21, 704, –720, –1163, 4127, 10784] / 2^{14}.

Table 2 Clock generator and front panel CLK connector.

Parameter	Condition	Min	Typical	Max	Unit
Connector type			SMA		
Internal clock reference					
Frequency			10		MHz
Accuracy			±3 ±1/year		ppm
Internal sampling clock generator					
Frequency			1000		MHz
External clock reference input (from front panel CLK connector)[5]					
Frequency		1	10	500	MHz
Frequency [6]	Jitter cleaner enabled	10 -10 ppm	10	500 +10 ppm	MHz
Frequency	Delay line used		10	100	MHz
Delay line tuning range[7]			500		ps
Signal level		0.5		3.3	Vpp
Input impedance	AC		50		Ω
Input impedance	DC		10k		Ω
Input impedance (high) [8]	AC		200		Ω
Clock reference output (on front panel CLK connector)[9]					
Frequency			10		MHz
Signal level	Into 50-Ω load		1.2		Vpp
Output impedance	AC		50		Ω
Output impedance	DC		10k		Ω
External direct sampling clock input (from front panel CLK connector)[10]					
Frequency			1000		MHz
Signal level		0.5		3.3	Vpp
Impedance	AC		50		Ω
Impedance	DC		10k		Ω

[5] Using a clock reference from an external source to synchronize the ADQ33 to the external source.
[6] The jitter cleaner requires the reference frequency to be a multiple of 10 MHz within ± 10ppm.
[7] Tuning of sampling clock phase relative to external clock reference input phase.
[8] Software-selectable high-impedance mode for bussed connection of multiple ADQ33.
[9] The internal clock reference of the ADQ33 is made available to synchronize external equipment.
[10] Using an external clock while bypassing the internal clock generator.

Table 3 Front panel TRIG connector

Parameter	Condition	Min	Typical	Max	Unit
Connector type			SMA		
Used as input (or GPIO)					
Impedance	DC		50		Ω
Impedance (high) [11]	DC		500		Ω
Signal level	50-Ω mode	-0.5		3.3	V
Adjustable threshold	50-Ω mode	0		2.8	V
Signal level	High impedance	-0.5		5.5	V
Adjustable threshold	High impedance	0		2.3	V
Pulse repetition frequency	As trigger			10	MHz
Time resolution	As trigger		125		ps
Update rate	As GPIO			62.5	MHz
Used as output (or GPIO)					
Impedance	DC		50		Ω
Output level high VOH	Into 50-Ω load	1.8			V
Output level low VOL	Into 50-Ω load			0.1	V
Pulse repetition frequency				62.5	MHz

Table 4 Front panel SYNC connector (may be used as a trigger source with larger timing grid)

Parameter	Condition	Min	Typical	Max	Unit
Connector type			SMA		
Used as input (or GPIO)					
Impedance	DC		50		Ω
Impedance (high) [11]	DC		500		Ω
Signal range	50-Ω mode	-0.5		3.3	V
Adjustable threshold	50-Ω mode	0		2.8	V
Signal level	High impedance	-0.5		5.5	V
Adjustable threshold	High impedance	0		2.3	V
Pulse repetition frequency	As trigger			10	MHz
Time resolution	As trigger		8		ns
Update rate	As GPIO			62.5	MHz
Used as output (or GPIO)					
Impedance	DC		50		Ω
Output level high VOH	Into 50-Ω load	1.8			V
Output level low VOL	Into 50-Ω load			0.1	V
Pulse repetition frequency				62.5	MHz

[11] Software-selectable high-impedance mode.

Table 5 Front panel GPIO connector

Parameter	Condition	Min	Typical	Max	Unit
Connector type			SMA		
Used as input					
Impedance			50		Ω
Impedance (high) [11]			10		kΩ
Input level high VIH		2			V
Input level low VIL				0.8	V
Update rate				62.5	MHz
Used as output					
Output Impedance			50		Ω
Output level high VOH	Into 50-Ω load	1.5			V
Output level high VOH	No load	3.2			V
Output level low VOL	Into 50-Ω load			0.1	V
Output level low VOL	No load			0.1	V
Update rate				62.5	MHz

Table 6 Custom GPIO expansion. See section 10.

Parameter	Value
Connector type	40-pin FFC/FPC connector, pitch 0.5 mm
Number of differential IO signals LVDS	8
Number of single-ended IO signals 3.3V	5

Table 7 Environment and mechanical parameters

Parameter	Condition	Min	Typical	Max	Unit
Power and temperature					
Power consumption [12]	FWDAQ		30		W
Power supply		10.8	12	13.2	V
Operating temperature	At fan inlet	0		45	ºC
Size					
Width			1		slot
Length			225.7		mm
Height			111.2		mm
Compliances					
RoHS3		Yes			
CE		Yes			
FCC	Exclusion according to CFR 47, part 15, paragraph 15.103(c).				

[12] Power consumption depends on firmware option and use case. Power consumption is measured during acquisition and streaming of data at 5 Gbyte/s to PC.

Table 8 Data acquisition

Parameter	Condition	Min	Typical	Max	Unit
Rearm time[13]				16	ns
Acquisition memory (Data FIFO)	Shared by all channels		8		Gbyte
Record length	Step size 1 sample	2		2^{32}-1	samples
Pretrigger[14]	Step size 8 samples	0		16 360	samples
Trigger delay[15]	Step size 8 samples	0		2^{35}-8	samples

Table 9 Data transfer[16]

Parameter	Value	Unit
Supported versions of data transfer standard PCIe	Gen1 / Gen2 / Gen3	
Supported number of lanes[17]	1 / 4 / 8	
Data rate to CPU sustained with headers	5	GByte/s
Data rate to CPU sustained without headers	7	GByte/s
Data rate to GPU sustained without headers	7	GByte/s
Data rate peer-to-peer to GPU sustained without headers	7	GByte/s

Table 10 Software support

Parameter	Value
Operating system[18]	Windows / Linux
GUI	Digitizer Studio
Example code	C, Python
API	C / C++

[13] Minimum time from the last sample of a record to the next trigger.
[14] Pre-trigger is set by assigning the parameter “horizontal offset” a negative value
[15] Trigger delay is set by assigning the parameter “horizontal offset” a positive value
[16] The parameters in this table represent the ADQ30 only. The system configuration including the PC may add other limitations.
[17] The ADQ33 must be installed in a 16 lanes slot or a slot with a connector with an open end.
[18] See 15-1494 Operating system support for a detailed listing of supported distributions.

4 FEATURES FOR DATA FLOW CONTROL, SYNCHRONIZATION AND PROCESSING

The ADQ33 features an advanced machine for flow control, synchronization, and signal processing. The block diagrams are shown in Figure 1 and Figure 2. The features are described in the following tables.

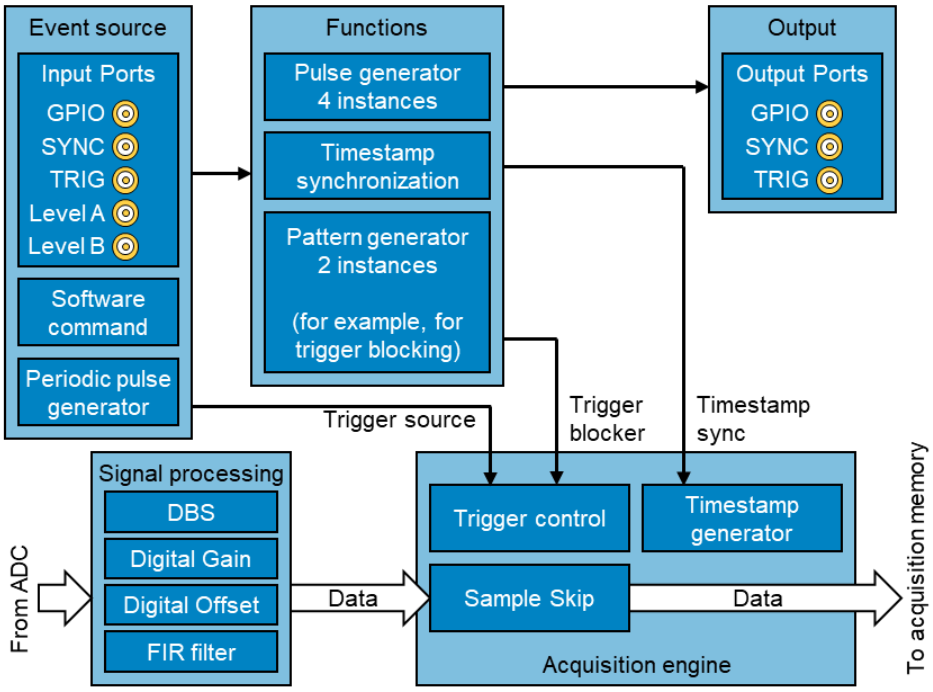


Figure 1 Flow control and synchronization block diagram.

Table 11 Digital signal processing blocks

Object type	Available selections
Digital Signal Processing Included signal processing in the data path for enhanced signal quality.	Digital Baseline Stabilizer (DBS) Digital gain Digital offset Digital FIR filter

Table 12 Flow control blocks

Object type	Available selections
Input ports Electrical connections to the ADQ33 for real-time operation (excluding the PCIe data interface) Used as event source.	Front panel TRIG Front panel SYNC Front panel GPIO Front panel CLK (clock reference or clock input only) Analog channel A Analog channel B
Event sources Signals for real-time control of activities in the firmware of ADQ33.	Software command External TRIG External SYNC External GPIO Internal periodic event generator Level analog channel A Level analog channel B
Functions Included operations for real-time control of activities in the firmware of ADQ33.	Pattern generator for timestamp synchronization Pattern generator general purpose, 2 instances Pulse generator, 4 instances
Output ports Electrical connections to the ADQ33 for real-time operation (excluding the PCIe data interface).	Front panel TRIG Front panel SYNC Front panel GPIO Front panel CLK (clock reference output only)

Table 13 Firmware functions for flow control

Function	Modes/selections	Event sources as stimuli
Pattern generator for timestamp synchronization Control the time of the ADQ33.		Software command External TRIG External SYNC Internal periodic event generator
Pulse generator (x4) Control output pulse shapes.	Rising edge Falling edge Pulse length Polarity	Software command External TRIG External SYNC Internal periodic event generator
Pattern generator general purpose (x2) For example, used for trigger blocking.	Once Window Gate Trigger counter	Software command External TRIG External SYNC Internal periodic event generator

Table 14 Firmware functions for acquisition

Function	Modes	Event Sources as stimuli / control
Trigger Initiate the acquisition of a data record.		Software command External TRIG External SYNC Internal periodic event generator Level analog channel A Level analog channel B
Data acquisition modes Configurations for sending digital data to the host PC.	Fixed record length Dynamic record length (zero suppression)	Selected **Trigger**
Data transfer modes Transport to CPU / GPU	Streaming with header Streaming without header	User set-up

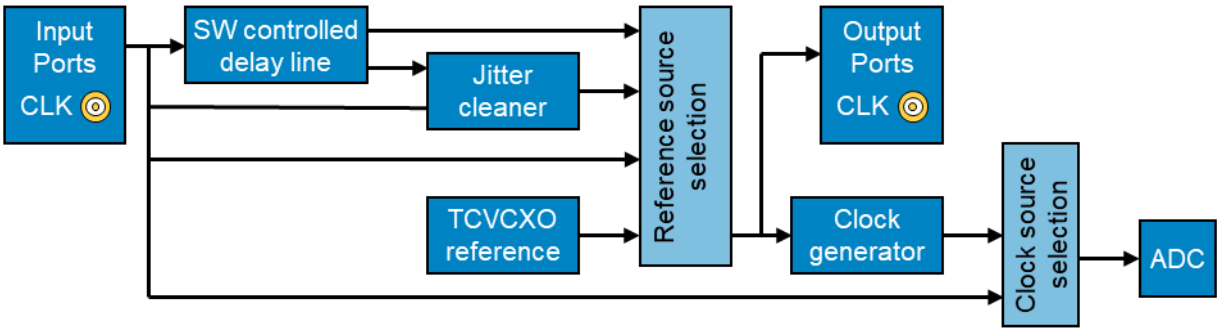


Figure 2 Clock generation block diagram.

Table 15 Clock generation

Function	Modes
Clock reference source Phase and frequency reference for the clock system.	Internal External External with jitter cleaner and/or delay line
Sampling clock sources Actual clock for taking the samples of the analog data.	Internal clock generator Direct external clock
Clock output	Selected clock reference

5 FIRMWARE

5.1 FWDAQ

The FWDAQ is always included with the ADQ33. The firmware includes control of the hardware and recording of data.

The dual-gain channel combination included in FWDAQ requires a separate license for ADQ33.

5.2 FWATD

The FWATD is optional. It includes thresholding for noise suppression and accumulations of waveforms. See datasheet 22-2912 for more details.

The dual-gain channel combination included in FWATD requires a separate license for ADQ33.

5.3 FWPD

The FWPD is optional. It includes detection and analysis of pulses. See datasheet 23-3028 for more details.

The dual-gain channel combination is included in FWPD requires a separate license for ADQ33.

5.4 Managing firmware

The digitizer supports multiple firmware images. Note the following about managing firmware images:

- The non-volatile memory on the digitizer can store up to four different firmware images (including the active firmware). Use the tool ADQAssist to change firmware and to upload new images to the digitizer.
- Each hardware can include a license for multiple firmware options. If all firmware images cannot be stored on the device, some may need be stored on the host computer for manual reprogramming via ADQAssist.
- The digitizer (and the enclosing host computer) must be power cycled for the firmware switch to be completed. This is required to let the PCIe bus enumerate with the new firmware.
- Some firmware features require a valid license key to activate. See the ordering information section for details about available firmware features.

6 ABSLOUTE MAXIMUM RATINGS

Table 16 Absolute maximum ratings

Parameter	Condition	Min	Max	Unit
Power supply to GND		-0.4	14	V
Operating temperature		0	45	ºC
Analog in to GND		-1.75	+1.75	V
TRIG to GND	50-Ω mode	-2	5	V
SYNC to GND	50-Ω mode	-2	5	V
TRIG to GND	500-Ω mode	-2	6	V
SYNC to GND	500-Ω mode	-2	6	V
CLK REF to GND AC amplitude			5	Vpp
CLK REF to GND DC-level		-5	5	V
GPIO to GND		-1.5	5	V
FFC / FPC differential signal to GND	Powered[19]	-0.5	2.3	V
	Not powered[19]	-0.5	0.5	V
FFC / FPC single-ended signal to GND [19]	Powered[19]	-0.3	3.8	V
	Not powered[19]	-0.3	0.5	V

Exposure to conditions exceeding these ratings may reduce lifetime or permanently damage the digitizer. The digitizer with PCIe format has a built-in fan to cool the device. The built-in temperature monitoring unit will protect the digitizer from overheating by temporarily shutting down parts of the device in an overheat situation.

The SMA connectors have an expected lifetime of 500 operations. For frequent connecting and disconnecting of cables, connector savers are recommended.

[19] The absolute maximum ratings depend on whether the ADQ33 is powered or not. It is recommended to use the respective power rail in the FFC connector to power or enable the external drivers to avoid driving overvoltage into an unpowered digitizer. Use the 1.8 V rail for the differential signals and 3.3 V for the single-ended signals.

7 TYPICAL PERFORMANCE

7.1 Frequency response

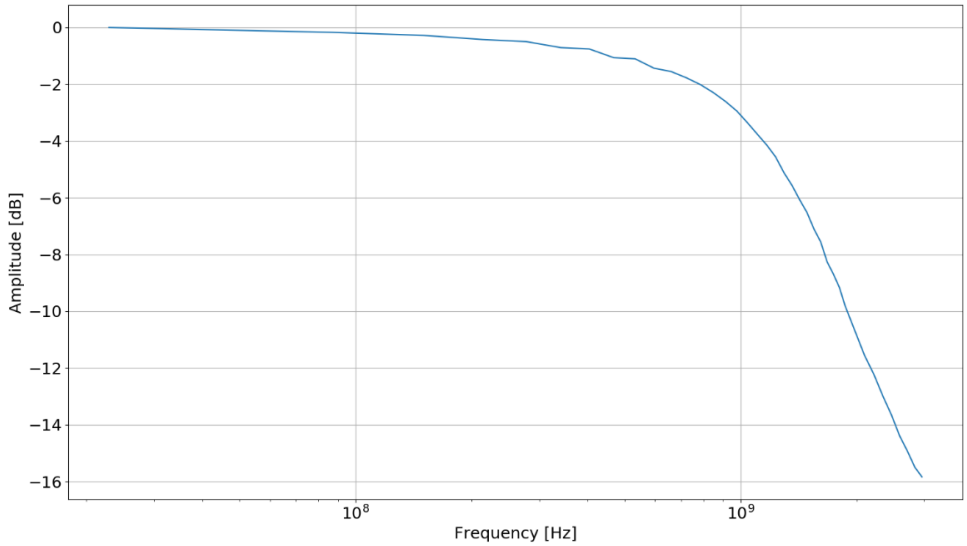


Figure 3 Frequency response, typical performance.

7.2 FFT

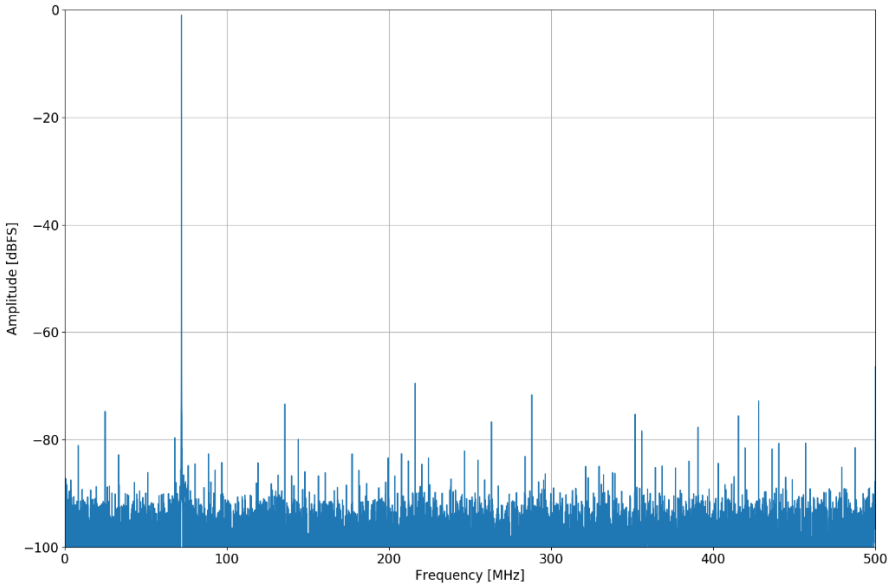


Figure 4 FFT typical single-tone performance.

8 BLOCK DIAGRAM

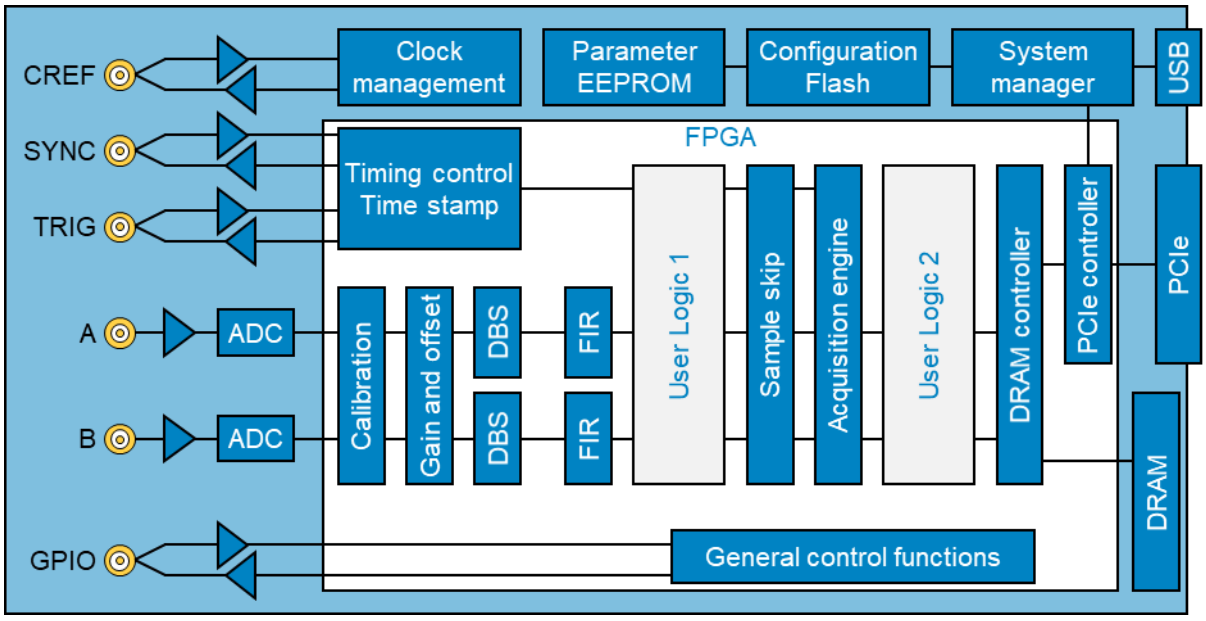
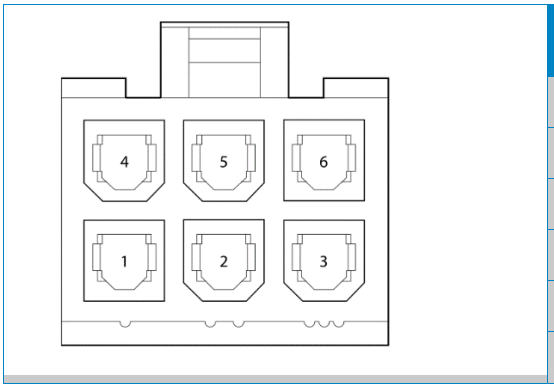


Figure 5 Block diagram.

Figure 5 shows a block diagram of ADQ33. The boxes “User Logic” are open for custom real-signal processing thought the firmware development kit (purchased separately).

9 HOST PC INTERFACE PCIE

The ADQ33-PCIe is powered from the power supply of the PC via a PCI Express 6-pin (2x3) auxiliary power supply connector. The connection in the cable should be as in Figure 6. A suitable connector is for example Molex 45559-0002. It is important that the auxiliary power supply is turned on immediately when the PC starts. Otherwise, the digitizer will not be recognized on the PCI Express bus.



Pin	Signal
1	+12 V
2	+12 V
3	+12 V
4	Ground
5	Sense (Ground)
6	Ground

Figure 6 Power supply connection. Cable connector, looking into the connector end.

10 GPIO EXPANSION

The FCP connector allows direct access to the FPGA for building custom expansion boards. The FCP connector requires custom firmware and is accessible through the FPGA development kit. The ADQ33 user guide document number 21-2539 contains a description of connector.

Note that this connector is connected directly to the FPGA. Damage caused by custom hardware failure is not covered by warranty.

Contact Teledyne SP Devices' sales representative for more information.

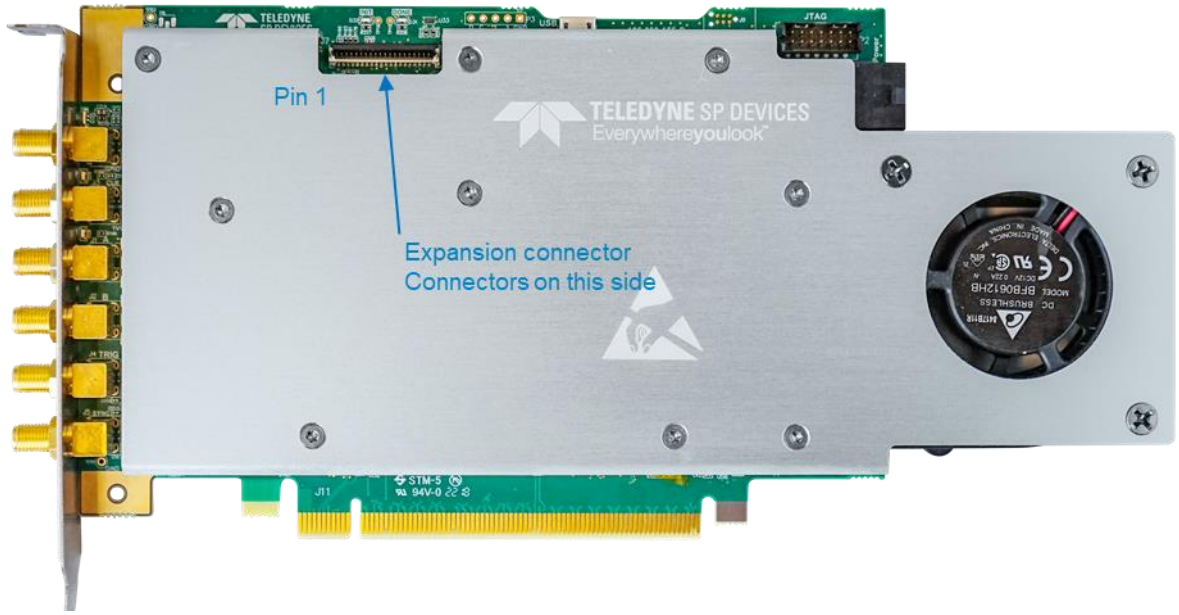


Figure 7 ADQ33 photo showing GPIO expansion connection on the top side.

11 MECHANICAL DRAWING

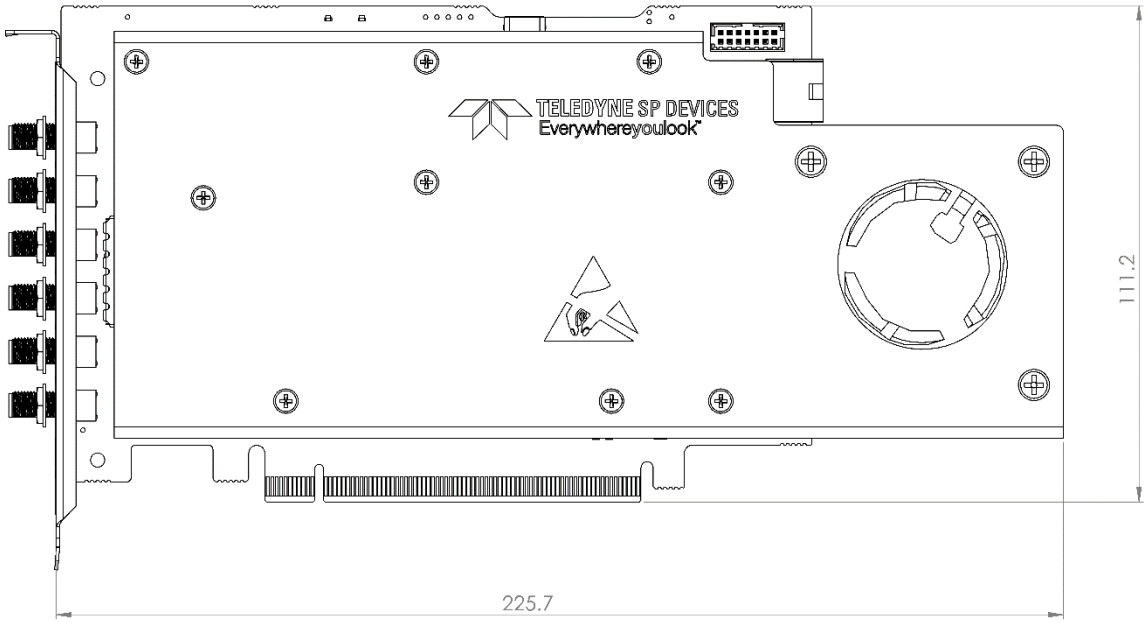


Figure 8 Mechanical drawing.

12 REFERENCES

Refer to TSPD's web site spdevices.com for the latest version of documents.

15-1494 Supported operating systems

18-2059 ADQUpdater user guide

20-2507 ADQ3 series development kit user guide

20-2521 ADQAssist user guide

21-2539 ADQ3 series user guide

22-2912 ADQ3 FWATD datasheet

23-3028 ADQ3 FWPD datasheet

23-3042 ADQ33-PDRX datasheet

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