SDR14TX Datasheet

SDR14TX is a dual channel arbitrary waveform generator:

- *2 analog channels*
- *2 GHz sample rate per channel*
- *First and second Nyquist operation up to 2 GHz*
- *14 bits vertical resolution*
- *1 GByte data memory*
- *Programmable data sequencing and markers*
- *Open FPGA for custom real-time applications*
- *Multi-unit synchronization*

SDR14TX Datasheet

Features

- 2 analog output channels
- 2 GHz sample rate per channel
- 14 bits vertical resolution
- Single-ended output
- Differential output
- Output impedance 50 Ω single-ended
- Output impedance 100 Ω differential
- DC – 1 GHz analog bandwidth
- 1 GHz – 2 GHz analog bandwidth
- Programmable DC-offset
- Internal / external clock reference
- Internal / external clock generation
- PXIe backplane clock reference
- External trigger for sequence control
- Multi-unit synchronization
- 1 GByte data memory
- Sequencing control
- Up to 16 384 segments
- Zero-insertion between segments
- Data interface PXIe and PCIe
- 31 individual markers per segment

Applications

- RADAR
- LIDAR
- Wireless communication
- Scientific instruments
- Particle physics
- Semiconductor test
- ATE
- Test and measurement
- Quantum technology
- Zero-IF IQ systems

Advantages

- Host PC form factor options for optimized system's partitioning.
- Advanced analog front-end and high sample rate for meeting system's requirements.
- Real-time custom processing solutions for advanced systems. This optimizes cost of ownership.
- SP Devices' design services are available for fast integration to lower time-to-market.

Flexible high performance waveform generation solution

The SDR14TX is a flexible arbitrary waveform generator (AWG) for high-speed transmission of arbitrary pulse signal as well as RF signals:

- The dual output enables transmission of 2 synchronized but independent waveforms. It also enable transmission of complex In-phase and Quadrature (I/Q) modulated signals.
- The DC-coupled analog output front-end is ideal for pulse data applications and for Zero-IF radio applications transmission.
- The high bandwidth enables direct transmission of RF and IF modulated signals in first or second Nyquist band (up to 2 GHz).
- The DC-offset tuning enables LO leakage suppression.
- The large on-board waveform memory, advanced sequencing engine and trigger capabilities enable pattern generation with precise timing.
- The trigger system allows for synchronization of multiple units.
- Differential or single-ended outputs for straightforward system integration.

Integrate into application

The SDR14TX comes with a software development kit to facilitate user's application development. SDR14TX supports Windows and the main Linux distributions.

Operating

The sequence of operation is

- Upload waveforms to the DRAM
- Set up sequencing
- Set up triggers
- Start the generation by triggering the SDR14TX

1 Preliminary technical data[1]

Table 1: General parameters

		SDR14TX
Key parameters		
Channels		2
Update rate / channel	[GHz]	2
Resolution	[bits]	14
Data memory	[GByte]	1
Power		
Power supply	[V]	12
Power dissipation	[W]	40
Trigger modes		
External		✓
Internal software		✓
Waveform segments [1]		
Segments		16 384
Segments length maximum	[MSamples]	250

1. See AWG application note 18-2066.

Table 2: Analog outputs, 1st Nyquist [1]

		SINGLE-ENDED	DIFFERENTIAL
Analog outputs			
Coupling		DC	DC
Output Impedance	[Ω]	50	100
Output range	[V_{pp}]	1	2
Bandwidth upper –3 dB [2]	[GHz]	1.0	1.0
Connector		1 x SMA	2 x SMA
Variable DC-offset			
Variable DC-offset range	[V]	±0.25	± 0.5
Analog performance			
Noise power spectral density	[dBm/Hz]	–152	–149
Full scale output power sine wave	[dBm]	4	10
SFDR[3] at Full Scale –1dB at 100 MHz	[dBc]	52	63
SFDR[3] at Full Scale –1dB at 300 MHz	[dBc]	52	56

1. Select Nyquist band by software command and design of analog reconstruction filter design.
2. Compensated for sinc-weight.
3. Including all tones and harmonics in the band DC to 1 GHz.

1. All values are typical unless otherwise noted.

Table 3: Analog outputs, 2nd Nyquist [1]

		SINGLE-ENDED	DIFFERENTIAL
Analog outputs			
Coupling		DC	DC
Output Impedance	[Ω]	50	100
Output range	[V_{pp}]	0.5	1
Bandwidth upper –3 dB	[GHz]	1.8	1.8
Bandwidth lower	[GHz]	1.0	1.0
Connector		1 x SMA	2 x SMA
Variable DC-offset			
Variable DC-offset range	[V]	±0.25	± 0.5
Analog performance			
Noise power spectral density	[dBm/Hz]	–152	–149
Full scale output power sine wave	[dBm]	–2	4
IM3 at Full Scale –7dB at 1500 MHz	[dBc]	50	50
IM3 at Full Scale –12dB at 1500 MHz	[dBc]	60	60

1. Select Nyquist band by software command and design of analog reconstruction filter design.

Table 4: Clock

		SDR14TX
Internal Clock Reference		
Frequency	[MHz]	10
External clock reference input		
Frequency	[MHz]	10
Signal level (min – max)	[Vpp]	0.5 – 3.3
Impedance AC	[Ω]	50
Impedance DC	[Ω]	10 k
Connector		MCX
Clock reference output		
Frequency	[MHz]	10
Signal level into 50 Ω load	[Vpp]	1.2
Output impedance AC	[Ω]	50
Output impedance DC	[Ω]	10 k
Duty cycle		50% ± 5%
Connector		MCX
External clock input		
Frequency	[GHz]	2
Connector		SMA

Table 5: External trigger

		SDR14TX
Input		
Impedance DC	[Ω]	50
Signal level (min – max)	[V]	–0.5 to 3.3
Adjustable trigger threshold	[V]	0 to 3
Time resolution	[ps]	500
Connector		MCX
Output		
Signal level output low max	[V]	0.1
Signal level output high min	[V]	2.2 (into 50 Ω load)
Impedance DC	[Ω]	50
Connector		MCX

Table 6: GPIO input/output for markers[1]

		SDR14TX
Connector		
Connector		Mini DSUB 9 way
Bi-directional signals		5
Input		
Impedance DC	[kΩ]	10
Signal level (min – max)	[V]	–0.5 to 3.3
Max GPIO data rate	[Mbit/s]	125
Output		
Impedance DC	[kΩ]	33
Signal level (min – max)	[V]	–0.5 to 3.3
Max GPIO data rate	[Mbit/s]	125

1. When set to output, the GPIO can be used for 31 individual markers per segment.

Table 7: General specifications

		–PXIE	–PCIE
Data rate			
Interface to host PC		PCIe	PCIe
Standard		Gen2 by 8 lanes	Gen2 by 8 lanes
Data rate peak[1]	[MBytes/s]	3400	3400
Waveform upload rate sustained[2]	[MBytes/s]	120	120
Mechanical			
Bus width mechanical	[lanes]	–	16
Weight	[g]	700	700
Board width	[slot]	2	2
Board length		–	short length
Board height		3U	–
Electrical			
Power supply		From chassis	6-pin ATX power
Bus width electrical	[lanes]	8	8
Temperature range			
Operation	[°C]	0 to 45	0 to 45
Compliances			
CE		✓	✓
RoHS2		✓	✓
FCC exclusion according to CFR 47, part 15, §15.103(c)		✓	✓

1. This is the peak capacity supported by a Gen2x8 PCIe interface.
2. This is the sustained data rate for uploading data from the host PC to the DRAM of the SDR14TX.

Table 8: Software support

	SDR14TX
Operating systems[1]	
Windows 7 32b and 64b	✓
Windows 8 / 8.1	✓
Windows 10	✓
Linux[2]	Kernel 2 and 3, main distributions
Application	
GUI [3]	ADCaptureLab
MATLAB [4]	API and examples
C/C++	API and examples
.Net (C#, Visual Basic)	API and examples
Python	Example scripts

1. Support is limited after OS manufacturers EOL.
2. Contact an SP Devices sales representative for information about currently supported distributions.
3. Windows only
4. Windows only

Baseband output

The full scale is according to **Table 2**.

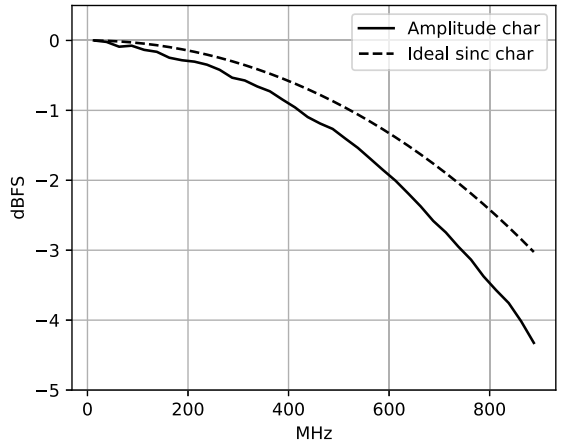


Figure 1: 1st Nyquist differential: bandwidth

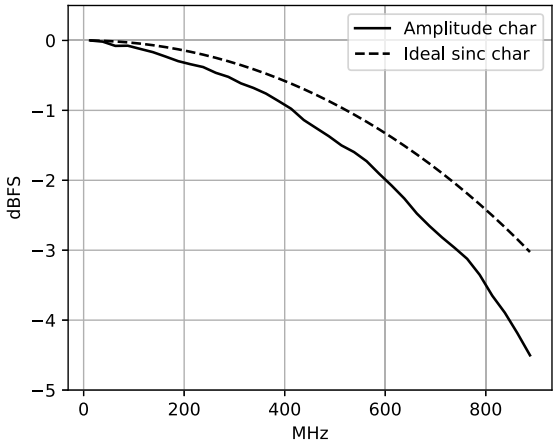


Figure 2: 1st Nyquist single-ended: bandwidth

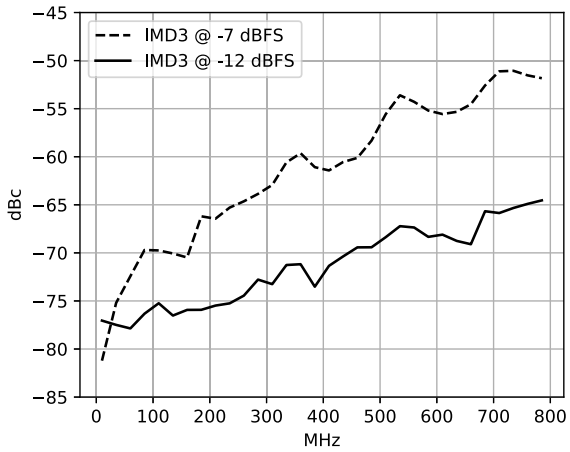


Figure 3: 1st Nyquist differential: IM3

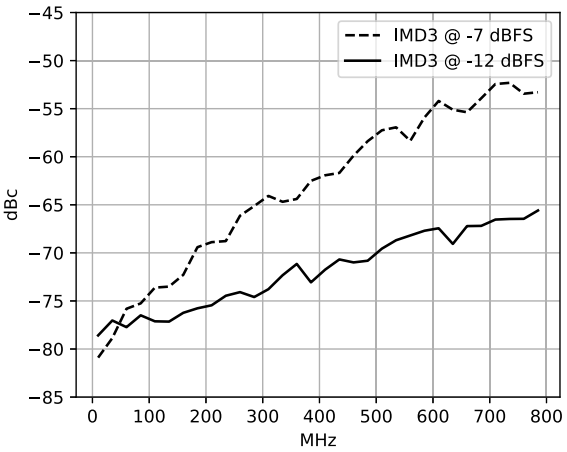


Figure 4: 1st Nyquist single-ended: IM3

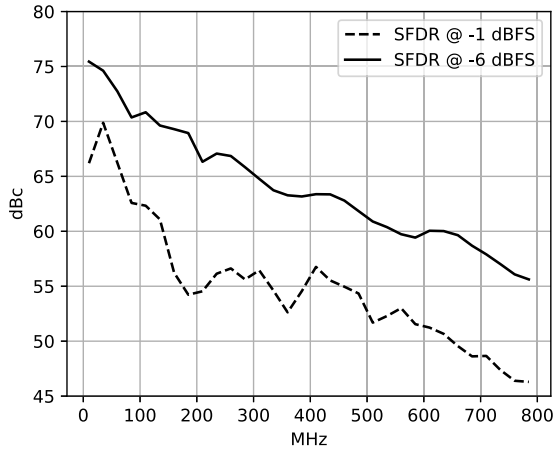


Figure 5: 1st Nyquist differential: SFDR

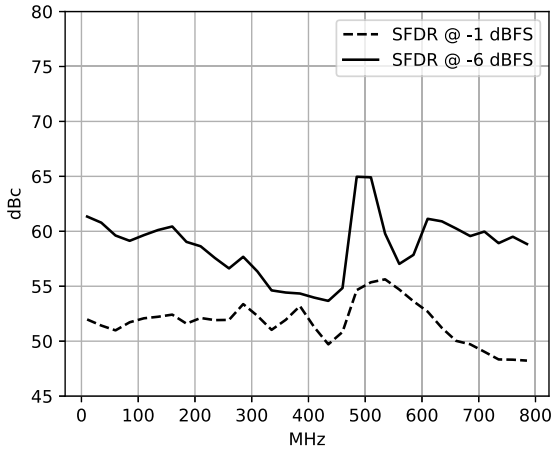


Figure 6: 1st Nyquist single-ended: SFDR

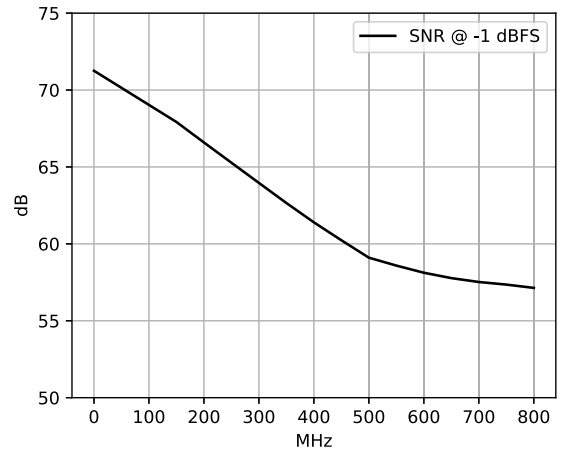


Figure 7: 1st Nyquist differential: SNR

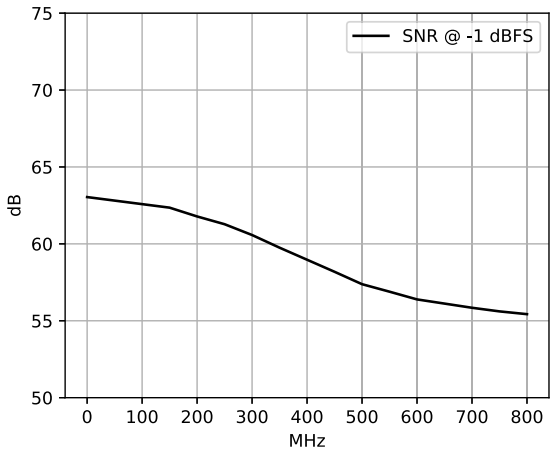


Figure 8: 1st Nyquist single-ended: SNR

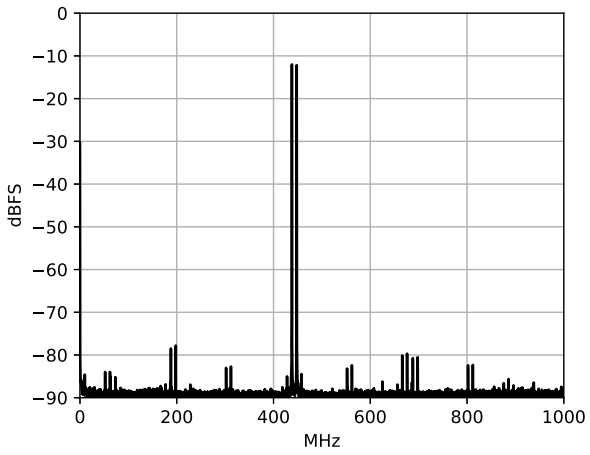


Figure 9: 1st Nyquist differential: FFT two-tone

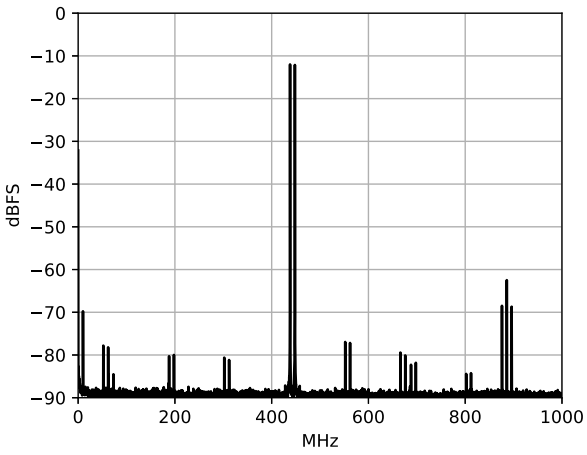


Figure 10: 1st Nyquist single-ended: FFT two-tone

RF output

The full scale according to **Table 3**.

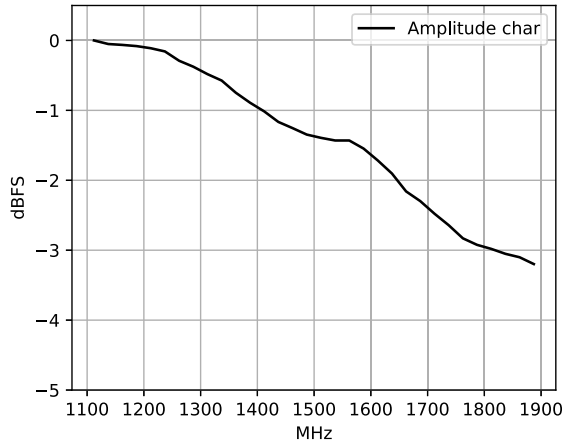


Figure 11: 2nd Nyquist differential: bandwidth

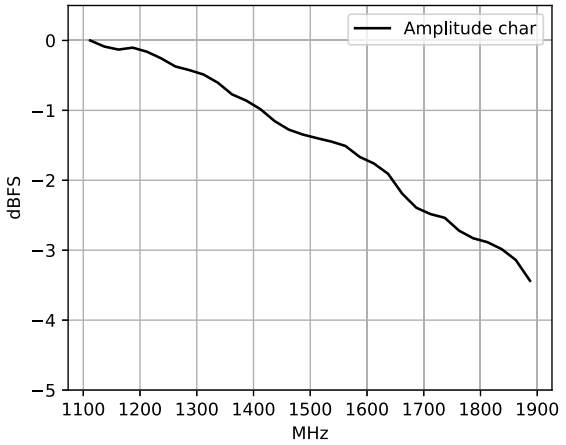


Figure 12: 2nd Nyquist single-ended: bandwidth

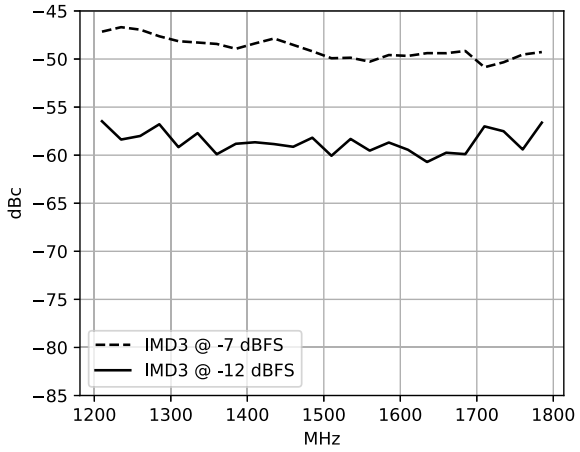


Figure 13: 2nd Nyquist differential: IM3

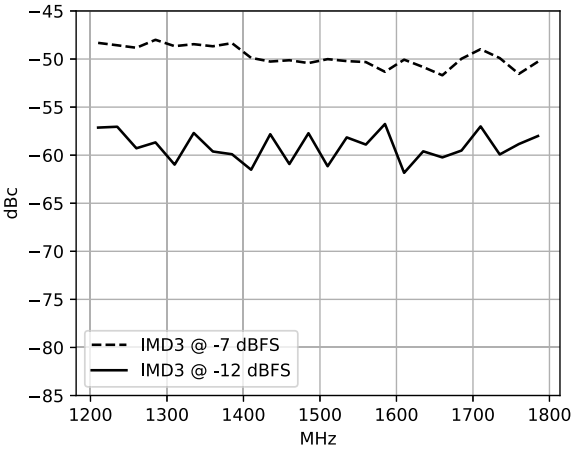


Figure 14: 2nd Nyquist single-ended: IM3

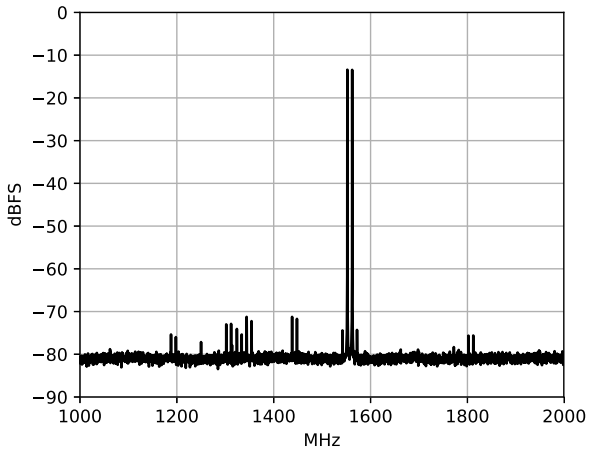


Figure 15: 2nd Nyquist differential: FFT two-tone

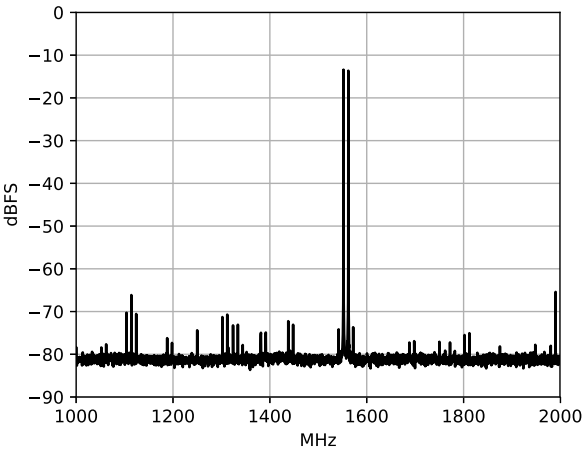


Figure 16: 2nd Nyquist single-ended: FFT two-tone

Test setup

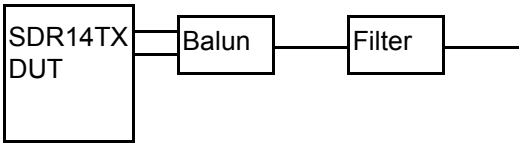


Figure 17: SDR14TX setup for differential measurements. Illustration of channel A only.

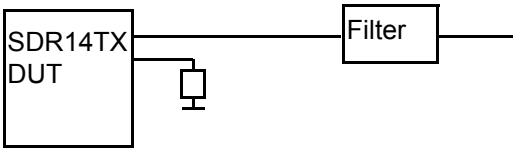
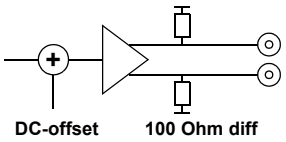


Figure 18: SDR14TX setup for single-ended measurements. Illustration of channel A only.

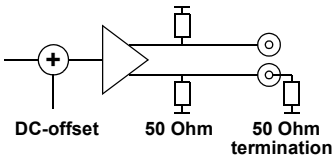
PART	MODEL	DESCRIPTION
DUT	SDR14TX	2 channel AWG
Balun	Marki BAL0003	Balun for measuring differential outputs
Filter	K&L Microwave 7L120-900/X2700-0/0	Low-pass reconstruction filter 900 MHz

2 Analog front-end



Differential output

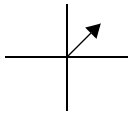
The DC-coupled analog front-end can be operated as a differential output. Each differential pair is available via two SMA connectors on the front panel.



Single-ended output

The DC-coupled analog front-end can be operated as a single-ended output. Use one of the differential outputs as a signal and terminate the other with a 50 Ohms termination.

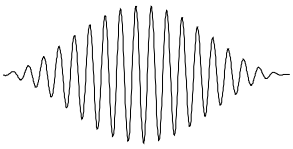
This is the default configuration. Use the 50 Ohms terminations supplied at delivery.



Baseband output

The DC-coupled analog front-end is designed for arbitrary wide-band general purpose waveforms. The dual outputs can also be used for I and Q zero-IF radio applications.

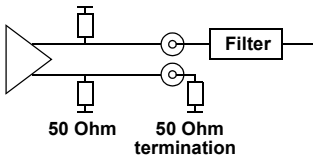
Select the baseband mode with a software command.



RF output

The analog front-end can be set to RF mode, where RF signals are generated in the second Nyquist band up to 2 GHz.

Select the RF mode with a software command.



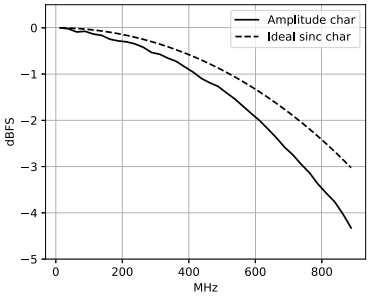
External filter required

The DC-coupled analog front-end is designed for flexible use case. There is thus no built-in reconstruction filter.

Select a low-pass filter for use in first Nyquist (DC–1 GHz).

Select a band-pass filter for use in first Nyquist (1 – 2 GHz).

Note that the frequency band indications include transition bands for the selected filters.

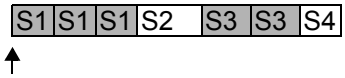


Anti-sinc filter required

The SDR14TX is designed to operate from pre-loaded records which are fed to the DACs from the large internal DRAM. Any required anti-sinc function should be applied when generating these waveforms before they are up-loaded to the SDR14TX.

Note that the anti-sinc filter differ depending on which Nyquist band that is selected.

3 Sequencing and synchronization



Segments and triggers

The memory of the SDR14TX can hold up to 16 384 different waveform segments. Each segments can be looped for a user-defined number of repetitions.

There are several possible trigger configurations that can be used for switching between segments. See application note 18-2066 for details.

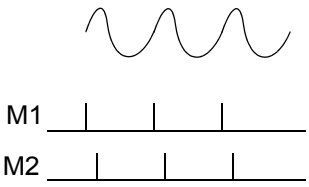
1	S1	200 x	Trig
2	S2	10 x	-
3	S1	1 x	-
4	S2	5 x	Trig

Playlist

There is a 1024-entry playlist table that optionally can be used to create a play order for the segment data. This allows changing the segment order quickly without having to reprogram the actual segment data. The playlist can also generate trigger outputs at specific positions. See application note 18-2066 for details.

Trigger input and synchronization

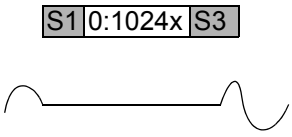
The segment sequencing can be controlled by an external trigger input. Multiple cards can be synchronized for a multi-channel AWG. See application note 13-0993 for details.



Marker generation and trigger output

There are several ways to generate markers and triggers.

- The internal trigger generator can trigger the sequences and produce a trigger output signal.
- The SDR14TX can generate 31 different markers on the 5 GPIO signals. These markers are programmed to follow the segment data.
- The play list function can generate triggers.



Zero generation

When there are long gaps in the data pattern, it is possible to encode commands into the data that will generate a set of zeros. In this way, silent periods in the signal will not waste segment data memory.

4 Form factor and data interface

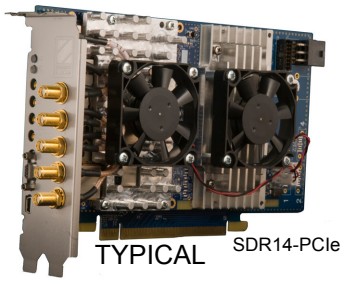
Modular instrumentation with cPCIe / PXIe (–PXIE)

- Modular instrumentation
- Synchronized channels

The cPCIe / PXIe form factor is intended for integration into a chassis for modular instrumentation or large scale acquisition. The SDR14TX can operate either in a Compact PCI Express or in a PXI Express chassis.

In a PXI Express chassis, the clock reference from the backplane can be used as clock reference for the digitizer. Backplane trigger is also supported to simplify integration.

Note that the backplane star trigger require a dedicated module in the timing slot of the chassis.



Systems integration with PCIe interface (–PCIE)

- All in one box
- High performance computing
- Cost-effective hardware

The PCIe form factor is used for integration into a host PC. The board is short length to enable compact solutions.

Note that the SDR14TX requires power from the ATX connector

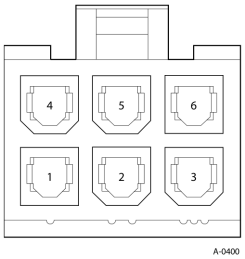


Figure 7-7: 150W-ATX Power Connector

Table 7-1: 150W-ATX Power Connector Pin-out

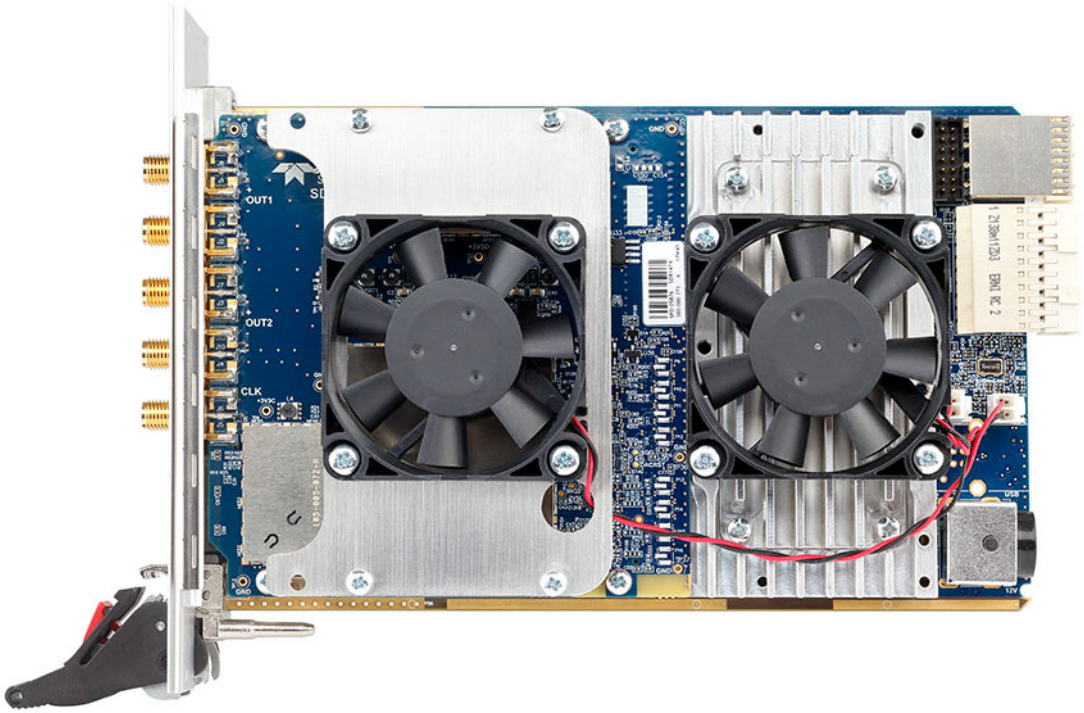
Pin	Signal
1	+12 V
2	+12 V
3	+12 V
4	Ground
5	Sense
6	Ground

Ordering information

ORDERING INFORMATION	
SDR14TX dual output AWG	SDR14TX
AVAILABLE OPTIONS	
Host PC interface PCI Express	–PCIE
Host PC interface PXI Express 3U chassis	–PXIE
RELATED PRODUCTS	
SDR14TX Development Kit	–SDR14TXDEVKIT

References

18-2066 Application Note AWG



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